



SHINRY 欣锐科技

success story

New Breakthrough in Full Topology HIL Simulation Testing for On-Board Chargers

A success story with SHINRY

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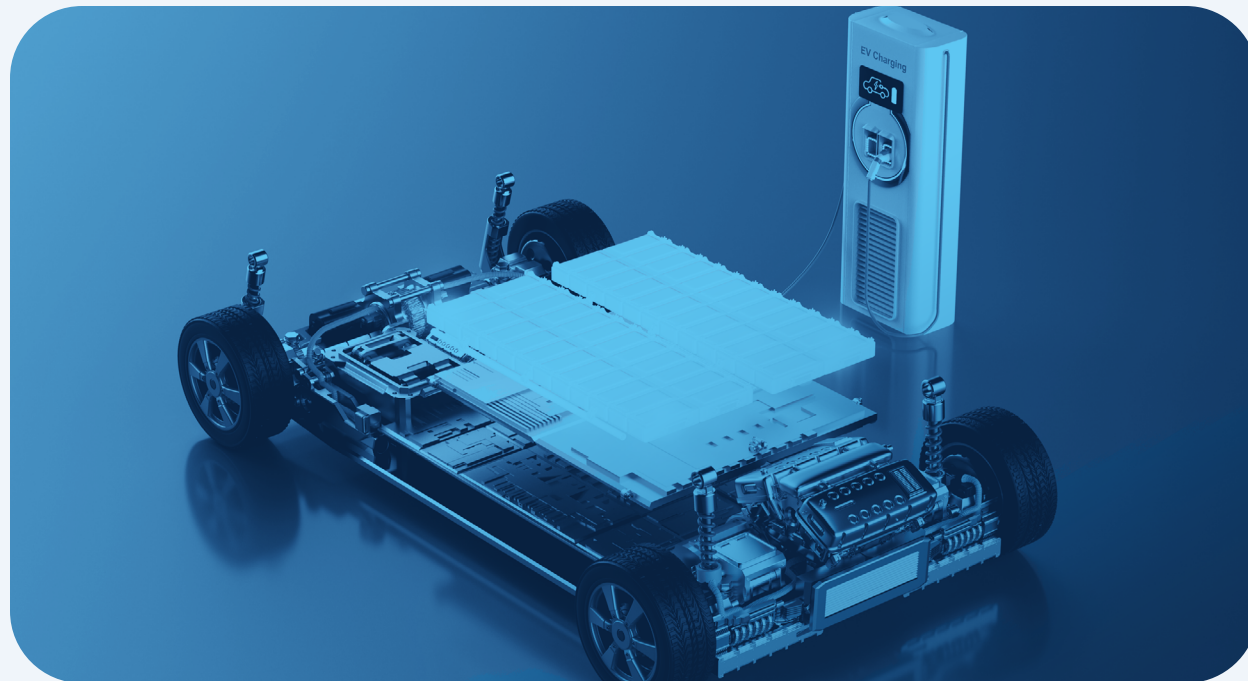


OPAL-RT
TECHNOLOGIES

SHINRY: China National High-Tech Enterprise in New Energy Vehicles

SHINRY Technologies Co., LTD. (referred to as SHINRY, stock code: 300745.SZ), founded in January 2005 in Shenzhen, the innovation capital of China, is a high-tech enterprise with three core business sections: EV, FCEV, and High-end Equipment. SHINRY provides high efficiency, high-power density, intelligence, and highly reliable power conversion systems to global customers.

Since entering the NEV industry in early 2006, SHINRY has focused on onboard power solutions for NEVs, with core technologies concentrated in onboard DC/DC converters, onboard chargers, and integrated products. SHINRY holds full independent intellectual property rights for its original core technologies in onboard power and supports many mainstream domestic and international vehicle models, making it a pioneer in the onboard power segment.



SHINRY has accumulated significant expertise in R&D and industrial applications in the fields of onboard power supplies, high-power charging, and hydrogen fuel cell vehicle DCF(DC/DC for Fuel Cell) products. With professional R&D innovation capabilities and engineering manufacturing capabilities, their company's product technology stands at the forefront of industry.

Starting in June 2025, SHINRY partnered with OPAL-RT China to explore the development of a hardware-in-the-loop (HIL) simulation test platform for the full topology of on-board chargers. The main products under test include high-frequency two-stage DC/DC circuits and bidirectional power high-frequency three-phase OBC circuits from mass production lines.

Wide Voltage Adaptation & Bidirectional Flow Control: What Sets OBC Apart

Compared to traditional new energy converters (such as motor drive inverters, DC charging pile modules, and wind-solar-storage converters), OBC (on-board chargers) has significant technical differences, primarily stemming from their unique application scenarios, functional objectives, and spatial constraints.

Wide Voltage Range Adaptation & High-Efficiency Resonant Topology

To accommodate different voltage standards (e.g., single-phase 220V / three-phase 380V) and cope with wide variations in battery voltage (e.g., from 200V to 800V platforms), the front-end AC/DC of the OBC must adapt to different grid inputs and provide a wide output voltage range. The back-end DC/DC typically employs resonant soft-switching topologies like LLC to achieve high efficiency across the full voltage and load range on the battery side (peak efficiency often required to exceed 95%). This is a key difference from inverters, which operate at relatively fixed operating points.

Bidirectional Energy Flow & Intelligent Power Management

Modern OBCs are evolving from unidirectional "grid-to-battery" charging to bidirectional charging/discharging (V2G/V2L) that includes "battery-to-grid/load". This requires the power topology (such as bidirectional LLC, bidirectional AC/DC) and control algorithms to support flexible, efficient, and safe bidirectional energy flow, as well as the capability to interact and intelligently schedule information with the grid or household loads.

The OBC has evolved from a single-function module into a complex power electronics system that integrates a bidirectional energy gateway, ultra-high-density integrated power supply, and smart grid interactive terminal. The core of its technical challenge lies in balancing three major goals under extreme physical constraints: bidirectional energy flow, ultimate efficiency and power density, and safety and reliability under all operating conditions. This represents the key difference in technical connotation compared to traditional converters with relatively single functions.

OBC HIL Testing: When 1+1>2

In the field of hardware-in-the-loop testing for on-board chargers, compared to simulating traditional large-scale electromagnetic transient models or simple unidirectional low-frequency power electronics topologies, the combination of HIL testing with OBC topology introduces a “1+1>2” level of complexity.



Simulation Models and Real-Time Performance

The main technical bottleneck here is: the three-phase LLC topology itself has a complex mathematical model with numerous switching state combinations. When operating at high frequencies of several hundred kHz, the simulation time step must be extremely short (typically < 100 nanoseconds) to accurately capture resonance processes, dead-time effects, and switching details. The addition of the DCDC stage makes the full-link model even larger, which pushes the real-time simulator’s computational power, FPGA resources, and model compilation optimization to its edge.



Mass-Produced Controllers: Black Box & Protection Coupling

Unlike developing “pre-research” controllers, using mature mass-produced control boards (rather than lab development boards) is key to being close to reality, but it also introduces uncertainties:

- Black Box Algorithms and Protection Logic: The internal control algorithms, protection thresholds, and response timing are not fully transparent. During HIL testing, any slight deviation from the behavior of the actual hardware could trigger unknown protection logic, leading to test interruptions or erroneous results.
- Interlinked Stringent Protections: Protection mechanisms such as overvoltage, overcurrent, overtemperature, and resonance anomalies react extremely quickly (microsecond level). Minor delays or errors in the simulation model or interface can be recognized as «faults» by the control board, preventing it from entering normal operating mode for testing.



High-Fidelity Signal Interaction and Interface

- Signal Injection at High-Frequency Switching Nodes: The control board needs to receive PWM feedback or status signals (such as primary side current/voltage) that accurately reflect the high-frequency switching actions (several hundred kHz). This requires the simulator interface to not only have sufficient bandwidth but also possess high noise immunity and signal integrity design to avoid false triggering from noise.
- Synchronous Measurement of Multiple High-Precision Channels: To monitor and verify full-link performance, it is necessary to synchronously collect multiple high-frequency voltage and current signals. This places high demands on the HIL test system’s synchronization accuracy, sampling rate, and number of I/O channels.

In response to SHINRY’s simulation requirements and the challenges mentioned above, especially to solve the simulation difficulties of LLC resonant circuits and ultra-high frequency switching devices, OPAL-RT China adopted the latest generation of FPGA hardware – the OP4800-IO series expansion units, and the eHS (FPGA-based power system and power electronics toolbox).

“When we used traditional simulation platforms to test the OBC three-phase LLC topology, it was difficult to accurately reproduce resonance anomalies under high-frequency switching, with unsatisfactory results.

The HIL solution provided by OPAL-RT can stably control the simulation time step within **190 ns** (minimum **110 ns**), and the capture accuracy of dead-time effects and switching losses can reach **90%**.

Based on this system, we identified **5 types** of hidden software and hardware integration problems in advance, further avoiding the risks and cycle losses of real vehicle testing.”

Engineer at SHINRY

eHS: FPGA-Based High-Speed & High-Performance Simulation Toolbox



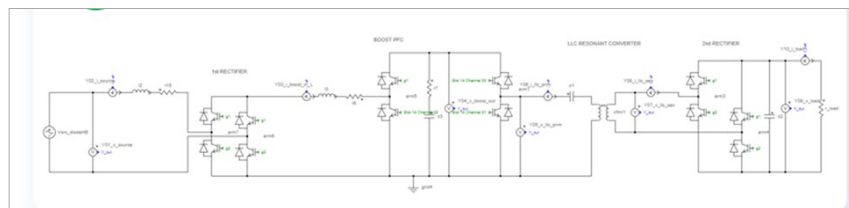
- ✓ Provides FPGA-based power electronics model solving computation functions and a rich set of motor models.
- ✓ Supports building highly customizable power electronics topology models.
- ✓ Supports receiving high switching frequencies: up to 500 kHz (250 kHz for resonant converter models).
- ✓ 625ps high sampling resolution (Oversampling technology).
- ✓ Solves computations at minimum nanosecond-level time steps.

With eHS, power electronics models running on the FPGA can be edited and modified without recompilation. After saving, they can be directly downloaded to the FPGA for execution, enabling the replacement of physical prototypes with digital power electronics topologies during testing, significantly enhancing testing efficiency and flexibility.



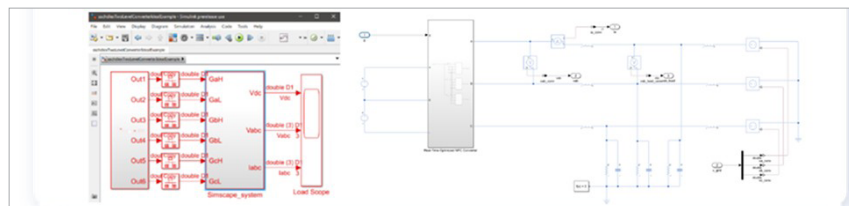
Physical Modeling & Flexible Topology

eHS is a general-purpose, reconfigurable power electronics solver embedded in the FPGA. It uses physical modeling rather than switching function models, allowing users to customize and modify the topology. eHS supports various graphical circuit simulations (OPAL-RT provides its proprietary Schematic Editor for FPGA model editing) or code generation via editing software. Users can arbitrarily add switching components in the schematic software and set parameters individually, modifying the FPGA model without going through a lengthy HDL code compilation process.



✓ Physical modeling

Displays each switching device and its parameters; no lengthy HDL compilation.



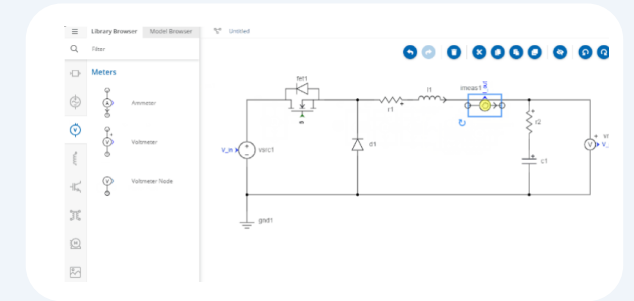
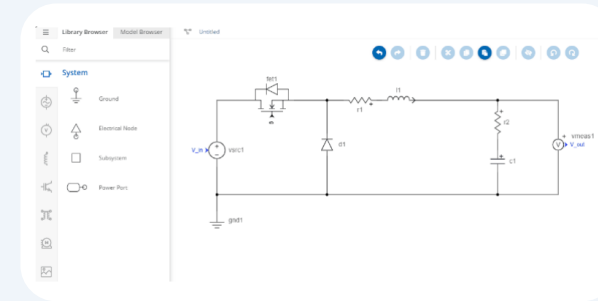
✗ Switching function modeling

Only shows subsystems and ports generated from HDL code.



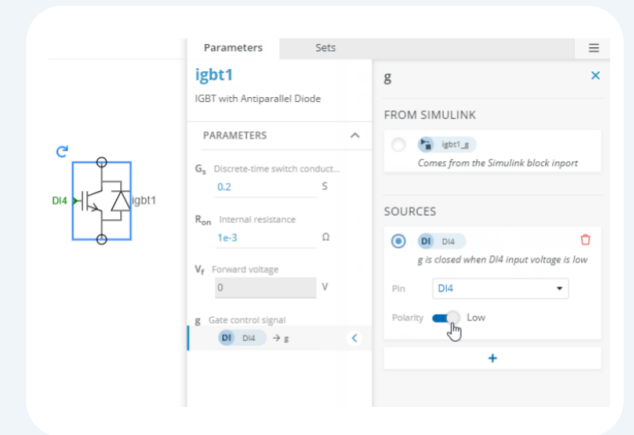
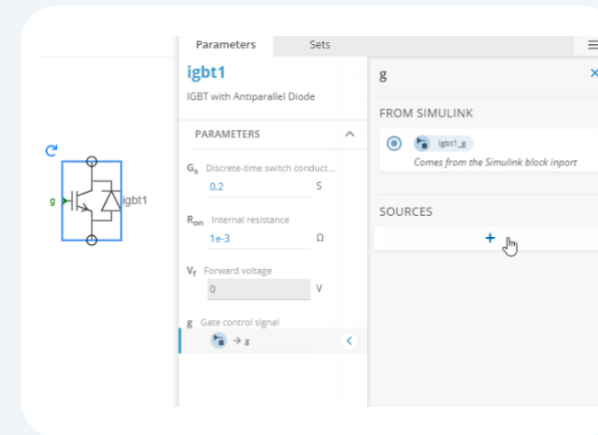
Graphical Drag-and-Drop Operation, Convenient and Efficient

In the Schematic Editor software, users can drag and drop components from the library into the circuit. The library includes modules such as RLC, controlled sources, switching tubes, circuit breakers, measurement points, transformers, and transmission lines. The operation is convenient and efficient, lowering the barrier to modeling.



Flexible Drive Configuration, Adapting to Actual PWM Signals

After dragging a switching tube into the topology, users can select the drive signal for the switching tube as an external Digital Input, feeding the actual PWM signal into the simulated power electronics switching device to drive the switch. It also allows configuration of the received drive signal as active-high, active-low, or setting intervals, timing, symmetry, and complementarity using the built-in FPGA PWM generator.

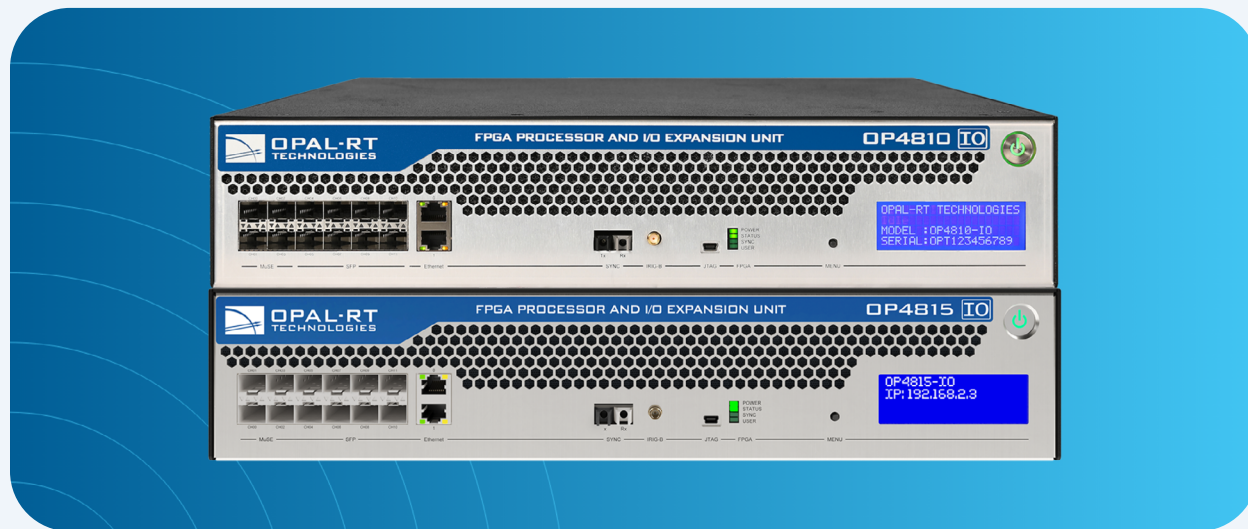


“We chose OPAL-RT’s solution primarily for its FPGA-based nanosecond-level real-time simulation, high-fidelity full-link model, and end-to-end closed-loop testing capabilities that support switching frequencies of several hundreds kHz — exactly what we needed to tackle the core technical challenges of OBCs and meet our demanding R&D requirements.”

Engineer at SHINRY

Empowering Complex Simulations with the OP4800-IO Series

The OP4800-IO series FPGA expansion units adopt the new generation AMD Versal series FPGA, a heterogeneous computing platform integrating a variety of computing resources including FPGA fabric, processing system (PS), and acceleration engines (AI engines and DSP engines). The Versal series introduces the concept of the Adaptive Compute Acceleration Platform (ACAP), with higher integration and flexibility, suitable for complex application scenarios such as AI inference, data center acceleration, and advanced communications.



Analog Output (AO) Performance

The AO on the OP4800-IO series FPGA expansion chassis features 10 MSPS sampling output, which can better adapt to the secondary side current output waveform corresponding to the high switching frequency (hundreds of kHz) of the LLC topology.

Closed-Loop Response and Computational Efficiency

Digital input channels receive pulse signals, and the DAC (AO channel, 10 MSPS) outputs voltage and current measurement point signals from the circuit. The closed-loop response cycle of the IO channels can be less than 1 microsecond. Excluding the hardware analog-to-digital conversion time, the FPGA model computation is in the hundreds of nanoseconds.

Key IO Channel Parameters (Configured OP48H10 High-Sampling Board as Example)

- ✓ High-Sampling AO Channels: 32 channels, 16-bits resolution, $\pm 10V$, sampling rate 10 MSPS.
- ✓ High-Sampling AI Channels: 32 channels, 16-bit resolution, $\pm 10V$, sampling rate 5 MSPS.
- ✓ Bidirectional Digital Channels: 64 channels, voltage range TTL 3.3V and 5V, supports software configuration of input or output direction, supports receiving PWM pulses with switching frequencies of 100 kHz and above.

High-Frequency Full-Link OBC HIL Test Solution

A comprehensive test system can identify software-hardware integration issues early, reducing real-vehicle failure risks—essential for developing high-performance, highly reliable in-vehicle power supplies.

The HIL test bench provided by OPAL-RT China for SHINRY accurately simulates the actual working environment of the OBC and DCDC, delivering full-process closed-loop testing including functional verification, fault simulation, and status monitoring. All indicators meet design specifications and industry standards.

Testing System		
OBC	Charge Mode	<ul style="list-style-type: none"> • Three-Phase Control Closed-Loop Test • Two-Phase Control Closed-Loop Test • Single-Phase Control Closed-Loop Test
	Precharge Mode	In Precharge mode, energy flows from the high-voltage battery side to the bus voltage side. The HIL bench needs to complete closed-loop testing of this function (charging of the high-voltage bus capacitor by the high-voltage battery) to ensure test coverage and controllability.
	V2X Modes	Includes: V2V, V2G, V2H, external V2L, internal V2L, Charge + internal V2L, external V2L + internal V2L, V2V + internal V2L, V2G + internal V2L, etc.
DCDC	Buck Mode	<ul style="list-style-type: none"> • LV Control Closed-Loop Test • MV Control Closed-Loop Test • LV+MV Control Closed-Loop Test
	Precharge Mode	In Precharge mode, energy flows from the LV side to the HV side; the low-voltage battery charges the high-voltage bus capacitor. The HIL bench needs to complete closed-loop testing of this function.
	Discharge Mode	In Discharge mode, the high-voltage bus capacitor rapidly releases energy through the PTC. The HIL bench needs to complete closed-loop testing of this function.
	LOCKED Mode	After a DCDC fault is activated, the controller enters LOCKED mode. The HIL bench needs to complete closed-loop testing of this function.
	Load Adaptability	Load adaptability supports electronic load CC, CV, CR mode simulation (load variation range 0-100% rated power), with adjustable rate, capable of supporting OBC and DCDC overshoot requirements during sudden load changes.
Automated Testing		
ISO26262 safety function specification	Extreme and demanding condition testing	

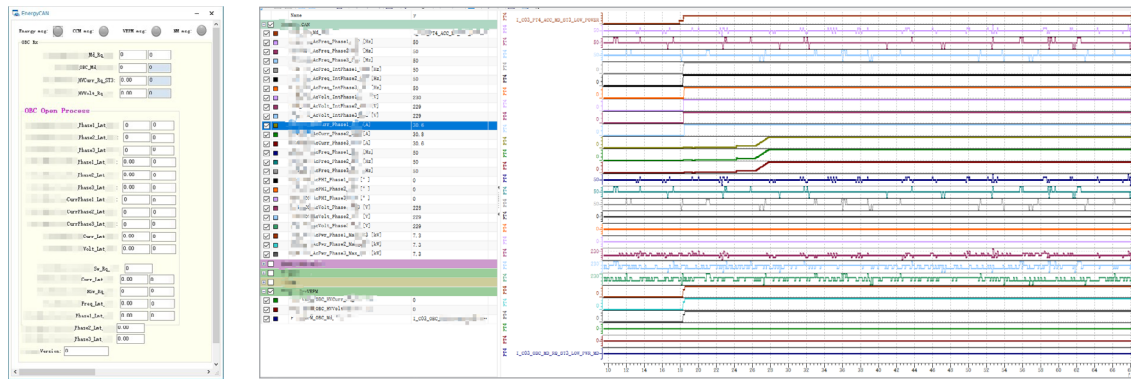
Flexible and Comprehensive Automated Testing System Empowers OBC Verification



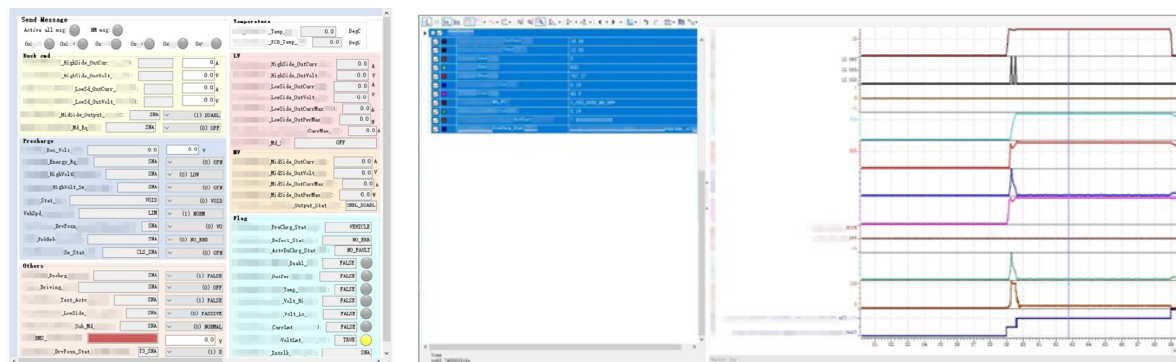
Full Test Process Automation, Improving Test Efficiency

All OBC test content can be completed through automated testing. In this project, the user's self-developed host computer in CANoe achieved simultaneous control, readback, and data logging functions for both the controller and the simulator. The host computer sends control commands to the simulator, which are parsed and fed into the model for parameter assignment and hardware device control. Simultaneously, the model sends back measurement point voltages and currents to the host computer via CAN messages for user monitoring.

OBC Host



DCDC Host



“The reuse of automated scripts has saved us a significant amount of repetitive work and greatly reduced manual operations. Previously, testing a single OBC model required at least 30 days; now it's shortened to 20 days. Both test accuracy and efficiency have achieved qualitative improvements.”

Engineer at SHINRY



Scalable and Reusable Test System, Maximizing Long-Term Value

In this case, the user continued using CANoe as the automated testing tool. All required control and observation quantities were built into the OBC with sufficient redundancy, not only meeting the current debugging needs but also considering potential future requirements, thus achieving “one-time debugging, long-term usability”.

After the automated test process is debugged, users can edit the test steps into automated test scripts according to test cases, enabling automated testing and reuse for later stages.



Open and Flexible Test Interface, Lowering the Barrier to Testing

RT-LAB provides open APIs such as Python and LabVIEW, allowing users to complete automated testing within their existing toolchains using familiar protocols. This eliminates the need for additional costs to learn new tools or replace existing equipment, significantly lowering the barrier to testing.



Supports Complex Test Scenarios, Improving Test Coverage

Supports CAN FD with a maximum bit rate of 8M, providing ample messages and strong support for independently controlling hundreds of relays for fault injection testing, enabling accurate reproduction of various extreme scenarios in the actual work of OBC.

SHINRY OBC Project Test Bench



Ready to innovate?

For over two decades, OPAL-RT TECHNOLOGIES has been a global leader in real-time simulation and hardware-in-the-loop (HIL) testing. Since 1997, OPAL-RT has empowered engineers and researchers with accessible, innovative, and customized simulation technology—bridging the gap between modeling and real-world applications. By leveraging high-performance computing, OPAL-RT accelerates the development of advanced solutions in energy, automotive, aerospace, and beyond. With our ISO 9001:2015 certification and a strong commitment to sustainable development, we're not just developing technology—we're building a better future, together.

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