

# Advancing EVSE Through Controller Hardware-in-the-Loop Validation

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#### **INTRODUCTION – GENERAL STRUCTURE**



#### FPGA model:

- Fast electrical circuit (user model)
- Runs in the FPGA (typical Ts<1  $\mu$ S)
- Is connected with the CPU model
- Is connected with hardware I/Os







#### CHIL and PHIL Setup at QEERI







## Controller Specs



03. Sync, LAN, CAN, RS-485 & Fiber Optics for Industrial Communication & Distributed Control System

04. Programming USB & High-Speed USB for Data Acquisition



06. Upto 68 I/Os Including 24 PWMs, 18 Analog Inputs, Quadrature Encoder, SPI, UART & I2C Interfaces

Buffer

06

Euffer

Sync

62

UART/PWM Interface

DI1-DI16

D01-D016

DI01-DI08

Fiber

Optics

IDC-40P Male

Connectors

#### $\geq$ R CH Ξ m 0 -R

02. High-Performance Dual-Core 480MHz (M7) /240MHz (M4) Microcontroller

SD

Card

eMMC 1-Bit Interfac

16-Bit Parallel Interface

SWD Interface

ULPI Interface

RMII Interface

6

ADC1

MAX11046

ADC2

MAX11046

a

S

AN17-AN18

ICP

**USB 2.0** 

PHY

Ethernet

AN1-AN8

05

AN9-A I

IDC-40P Male

Connector

5" Capacitive Touch Display 800x480

24-E t RGB Interface, I2C Touch Interface 

STM32H745BI

**CAN Interface** 

160

IDC-40P Male Connector

CAN

UART

**RS-485** 

6

COMM

SPI, UART & I2C Inte

02



## Considered System

#### DC EVSE





#### Control Technique







(e) (f) Block diagrams of existing control methods for three-phase active front-end rectifier with LCL filter. (a) grid current feedback, (b) rectifier current feedback, (c) grid current and rectifier current feedbacks, (d) rectifier current, capacitor current and capacitor voltage feedbacks, (e) rectifier current and capacitor voltage fee



Block diagram of the proposed current sensorless control technique

#### Control Technique



#### System And Control Parameters

Description and Symbol	Value
Grid voltage amplitude, $E_m$	$120\sqrt{2} V$
DC-link voltage reference, $V_{dc}^*$	400V
Grid-side inductance, $L_{g}$	2.5mH
Rectifier-side inductance, $L_r$	5mH
Inductor resistances, $R_g$ and $R_g$	0.4Ω, 0.5Ω
Filter capacitor, C	22µF
DC capacitors, $C_1 = C_2$	470µF
Load	40 Ω - 80 Ω
Virtual damping resistor, $R_d$	8Ω
PI gains, $K_p$ and $K_i$	0.04, 10
Sampling period: $T_s$	40µs







Steady-state responses of dc- and ac-side variables under balanced grid.



Steady-state responses of dc- and ac-side variables under unbalanced grid.



Steady-state responses of dc-and ac-side variables under distorted grid.









Responses of dc-and ac-side variables for a step change in  $R_d$  from 8  $\Omega$  to 0  $\Omega$ .



Dynamic responses of dc-and ac-side variables for a step change in load resistance from 80  $\Omega$  to 40  $\Omega$  and  $V_{dc}^*$  from 400V to 450V.









 $u_{q,sw} = \frac{2L_r k_1}{V_{J_1}} \Big( k_2 e^{k_3 \sigma_q} - 1 \Big)$ 

H. Komurcugil, S. Bayhan, N. Guler and H. Abu-Rub, "A New Exponential Reaching Law Approach to the Sliding Mode Control: A Multilevel Multifunction Converter Application," in IEEE Transactions on Industrial Electronics, vol. 70, no. 8, pp. 7557-7568, Aug. 2023, doi: 10.1109/TIE.2022.3229369.



 $u_{d,sw} = \frac{2L_r k_1}{V_r} \Big( k_2 e^{k_3 \sigma_d} - 1 \Big)$ 



Waveforms for scenario 1. (a) Non-distorted and balanced grid, (b) Distorted and balanced grid, (c) Non-distorted and unbalanced grid.  $e_{ga}$ ,  $e_{gabe}(200 \text{ V/div})$ ,  $i_{ga}$ ,  $i_{gabe}$ ,  $i_{ra}$ ,  $i_{La}(20 \text{ A / div})$ , and  $V_{de}$ ,  $V_{C1}$ ,  $V_{C2}(250 \text{ V / div})$ .



Waveforms for scenario 2. (a) Non-distorted and balanced grid, (b) Distorted and balanced grid, (c) Non-distorted and unbalanced grid.  $e_{ga}$ ,  $e_{gabe}(200 \text{ V/div})$ ,  $i_{ga}$ ,  $i_{gabe}$ ,  $i_{ra}$ ,  $i_{La}(20 \text{ A / div})$ , and  $V_{de}$ ,  $V_{C1}$ ,  $V_{C2}(250 \text{ V / div})$ .





Waveforms for scenario 3. (a) Non-distorted and balanced grid, (b) Distorted and balanced grid, (c) Non-distorted and unbalanced grid.  $e_{ga}$ ,  $e_{gabe}$  (200 V/div),  $i_{ga}$ ,  $i_{gabe}$ ,  $i_{ra}$ ,  $i_{La}$  (20A / div), and  $V_{dc}$ ,  $V_{C1}$ ,  $V_{C2}$  (250V / div).



Waveforms for scenario 4. (a) Non-distorted and balanced grid, (b) Distorted and balanced grid, (c) Non-distorted and unbalanced grid.  $e_{ga}$ ,  $e_{gabe}$  (200 V/div),  $i_{ga}$ ,  $i_{gabe}$ ,  $i_{ra}$ ,  $i_{La}$  (20A / div), and  $V_{de}$ ,  $V_{C1}$ ,  $V_{C2}$  (250V / div).



### Conclusion

- □ C-HIL validation is a transformative approach that holds immense promise in advancing the development of power electronic converters for EVSE.
- □ C-HIL validation accelerates development processes by facilitating rapid prototyping and optimization of control algorithms, resulting in more efficient and reliable converter designs.
- □ It contributes to the creation of robust and resilient converter designs by evaluating controller responses to fault conditions, ensuring adaptability to unforeseen challenges.
- □ The validation method supports bidirectional power flow control, paving the way for advanced functionalities like vehicle-to-grid (V2G) services and efficient energy management.
- By bridging the gap between theoretical models and physical prototypes through hardware integration, C-HIL validation enhances the accuracy of converter testing and validation.









