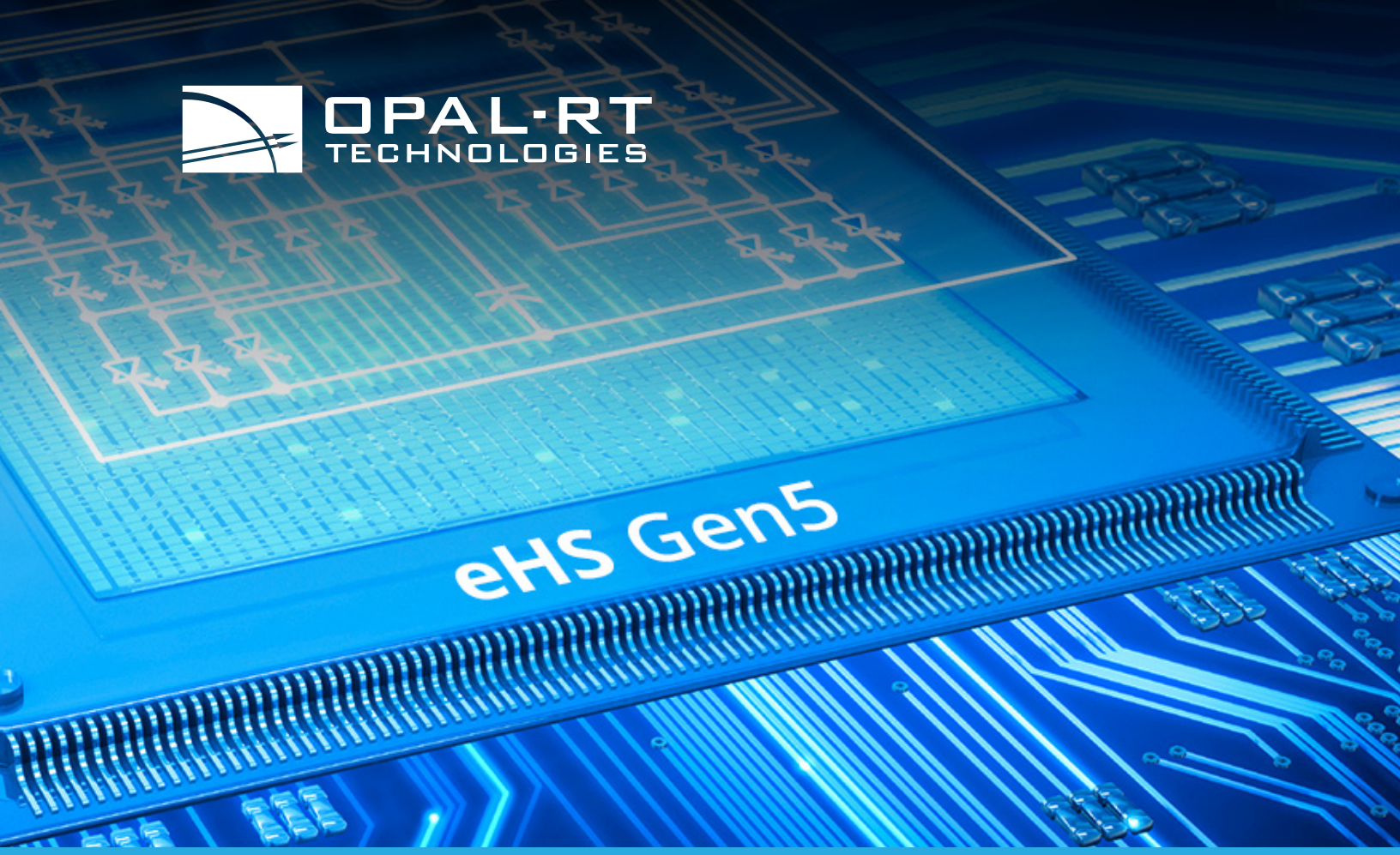


eHS Gen5: Unveiling the new solver of the fastest FPGA- Based Power Electronics Toolbox in the industry

As the world electrifies, researchers are pushing the limits of power electronics requirements in terms of efficiency and power density. OPAL-RT has been at the **forefront of FPGA simulation for over 20 years** and continues to innovate to meet the demands of the power electronics industry.

eHS Gen5 offers outstanding simulation speed and accuracy, for a wide range of high-frequency converter applications. Its **90ns time step and 625ps gate pulse sampling resolution** make it ideal for real-time simulation of user-defined resonant converter topologies.

eHS simplifies FPGA usage for HIL simulation, without the need for coding or mathematical modeling. It's the perfect tool for transitioning from circuit design to FPGA implementation.

REDEFINING SPEED, POWER AND ACCURACY OF REAL-TIME FPGA SIMULATIONS

The new generation of eHS is now faster and more efficient than ever before! Explore the highlights of eHS Gen5 that will take innovation to the next level.

No decoupling

Avoid instabilities and the manual struggles of artificially decoupling networks. Run up to 21 3-phase converter models (128 switches) or 250 grid nodes @ 500 ns on the same FPGA core.

FPGA cores scaling

Have larger models or need to run faster? Efficient parallelization algorithms ensure you can connect multiple FPGA-based simulators.

Picosecond Oversampling

625ps oversampling with interpolating converter models ensures the highest sampling resolution and accuracy available.

Co-simulation ready

Combine performance and capability, reserving the FPGA for high-frequency switching modeling, and CPU for larger network system simulation.

STREAMLINED USER INTERFACE

A modern Schematic Editor facilitates modelling of power electronics and assignment of analog/ digital I/Os. Integrated with Simulink and HYPERSIM, controls can also be virtualized for Software-in-the-Loop (SIL) testing.

Button Header

Complete diagram actions quickly and easily.

Button Header

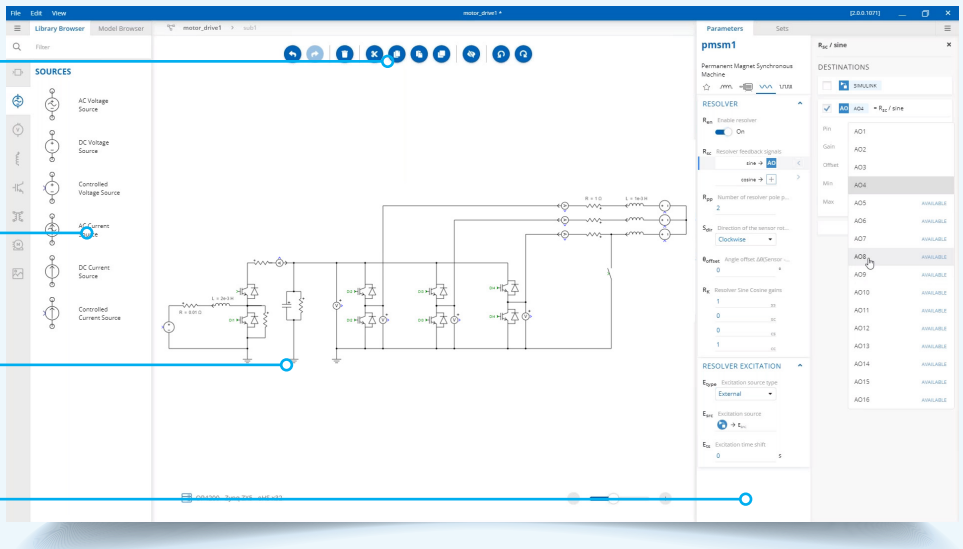
Complete diagram actions quickly and easily.

Work Area

Easily assemble and manipulated models.

Parameters Side Bar

Edit parameters of the selected components.



FPGA-BASED POWER ELECTRONICS TOOLBOX
A VERSATILE SOLUTION FOR DIVERSE APPLICATIONS

The FPGA-Based Power Electronics Toolbox covers a wide range of applications, from EV onboard chargers to renewable energy conversion, or even highly complex modular multilevel converters.

Its libraries contain both individual components and optimized readily available converter and machine models, some with embedded fault capability. For example, the parameter sets feature of eHS can support an unlimited number of test cases, as it allows endless variations of parameters and fault injections at every stage of the power electronics circuit.

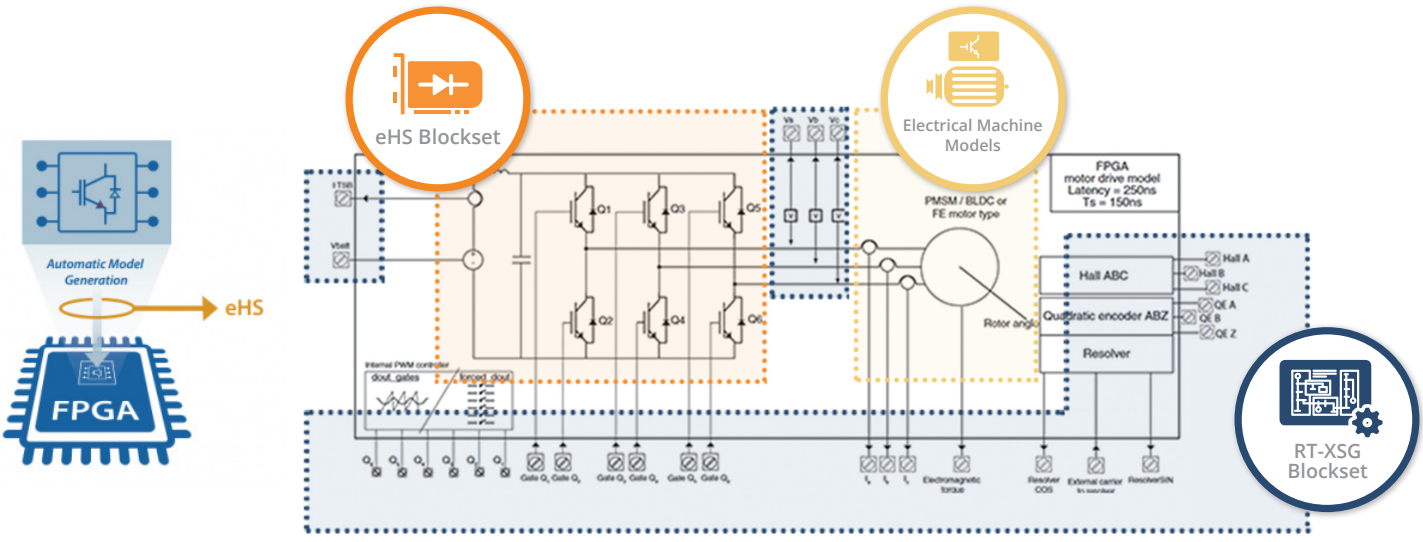
The FPGA-Based Power Electronics Toolbox is comprised of three key software technologies: eHS Blockset (including electrical machine models), RT-XSG Blockset and MMC Blockset.

eHS Blockset

Converters (2-level HB, 3-level NPC, among others), **electrical machine** models (induction, permanent magnet, among others), transformers, lines and more are readily available to quickly create circuit designs, directly from the schematic editor.

RT-XSG Blockset

Have more specific needs? RT-XSG is a development kit integrated into Simulink. It opens-up the FPGA design and allows users to implement optimized models that could run at 20ns steps and be connected to the eHS core. OPAL-RT also offers custom IP delivery services tailored to your needs.



MMC Blockset

A specialized technology providing various submodule topologies (half-bridge, full-bridge, T-type, among others) enabling Rapid Control Prototyping of new MMC control and protection schemes as well as evaluating interactions between vendors and large-scale power system.

OPAL-RT TECHNOLOGIES

FPGA-BASED POWER ELECTRONICS TOOLBOX
TECHNICAL SPECIFICATIONS

Features	eHS Blockset	RT-XSG Blockset	MMC Blockset
Targeted applications	High flexibility workflow for most power electronics applications	High performance solution for customized and optimized applications	Specialized technology for multilevel VSC converter simulation
Targeted platforms	OP4512 (Kintex™ 7 410T) OP4610XG (Kintex™ 7 410T) OP5707XG (Virtex™ 7 485T)		
Supported component types	Switches, converters, machines, RLC, transformers, lines, sources, among others	Implement your own digital equation on the FPGA device using the System Generator for DSP library of Xilinx	Submodule types: • Half-bridge, full-bridge, Clamped-double, T-type, among others • Mixed types of submodules in a valve is possible
Component capacity per FPGA	• 128 electrical sources • 128 measurements • 128 switching devices • 344 states* • Up to 4x 6-phase electrical machines **Overall capability:** • Up to 21 converter models • Up to 21 DER models • 250-node grid @ 500 ns	• Capacity is FPGA and implementation dependent • Access up to 256 simulator I/Os • Scale easily to multiple FPGAs using Aurora high speed links	• 500 submodules per valve • 6 valves per converter • 3 converters with voltage balance control (VBC) or • 2 converters with voltage balance control (VBC) and SFP connection to external control
Minimum time step	90ns	20ns	100ns
Maximum switching frequency	500kHz**	N/A	100kHz
Sampling rate	625ps oversampling	5ns	100ns
Maximum number of parameters sets	Unlimited***	N/A	
Compatible circuit editors	Simscape Specialized Power Systems, PLECS, PSIM and OPAL-RT Schematic Editor	Simulink with Xilinx System Generator	Simulink

* Estimated value. The maximum number of states depends on the number of inputs and outputs that need to be computed as well. There is no hardcoded limit.
**250kHz for resonant converter models and up to 500kHz for VSC applications. For higher requirements, slower than real-time modelling with parameter scaling is available, or a RT-XSG custom FPGA model implementation could be coupled with the eHS core.
*** Unlimited when using CPU buffered parameter sets. 512 when using FPGA buffered parameter sets.