



Systematic Characterization of Power Hardware-in-the-Loop Evaluation Platform Stability

Preprint

Jing Wang, Blake Lundstrom, Ismael Mendoza,
and Annabelle Pratt

National Renewable Energy Laboratory

*Presented at the 2019 IEEE Energy Conversion Congress and Exposition
(IEEE ECCE)*

Baltimore, Maryland

September 29-October 3, 2019

**NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC**

This report is available at no cost from the National Renewable Energy
Laboratory (NREL) at www.nrel.gov/publications.

Contract No. DE-AC36-08GO28308

Conference Paper
NREL/CP-5D00-73162
December 2019



Systematic Characterization of Power Hardware-in-the-Loop Evaluation Platform Stability

Preprint

Jing Wang, Blake Lundstrom, Ismael Mendoza, and Annabelle Pratt

National Renewable Energy Laboratory

Suggested Citation

Wang, Jing, Blake Lundstrom, Ismael Mendoza, and Annabelle Pratt. 2019. *Systematic Characterization of Power Hardware-in-the-Loop Evaluation Platform Stability: Preprint*. Golden, CO: National Renewable Energy Laboratory. NREL/CP-5D00-73162. <https://www.nrel.gov/docs/fy20osti/73162.pdf>.

© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

**NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC**

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Contract No. DE-AC36-08GO28308

Conference Paper
NREL/CP-5D00-73162
December 2019

National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, CO 80401
303-275-3000 • www.nrel.gov

NOTICE

This work was authored by the National Renewable Energy Laboratory, operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding provided by U.S. Department of Energy Office of Electricity, Advanced Grid Research and Development. The views expressed herein do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

U.S. Department of Energy (DOE) reports produced after 1991 and a growing number of pre-1991 documents are available free via www.OSTI.gov.

Cover Photos by Dennis Schroeder: (clockwise, left to right) NREL 51934, NREL 45897, NREL 42160, NREL 45891, NREL 48097, NREL 46526.

NREL prints on paper that contains recycled content.

Systematic Characterization of Power Hardware-in-the-Loop Evaluation Platform Stability

Jing Wang, Blake Lundstrom, Ismael Mendoza and Annabelle Pratt
National Renewable Energy Laboratory, Golden, CO 80401 USA

jing.wang@nrel.gov, blake.lundstrom@nrel.gov, ismael.mendoza@nrel.gov, annabelle.pratt@nrel.gov

Abstract—This paper presents a systematic approach to characterize the stability of a power-hardware-in-the-loop (PHIL) platform, an important step in PHIL tests. Many existing works focus the stability assessments on the PHIL interface algorithm; however, this work considers all software and hardware subsystems that form the closed loop of the PHIL experiment and develops a complete closed-loop stability assessment. This assessment is developed in the context of a common framework that can be readily applied to other PHIL platforms. This paper presents methods for characterizing key PHIL subsystems toward obtaining transfer functions to be used for analysis. The systematic stability assessment approach is demonstrated for a case study involving PHIL testing of a solar inverter and validated using experimental data.

Keywords—Stability assessment, Interface Algorithm, Power-hardware-in-the-Loop (PHIL).

I. INTRODUCTION

Power-hardware-in-the-loop (PHIL) testing has been widely used as an important evaluation method for integrating distributed energy resources (e.g., solar inverters) into electricity grids before site commissioning [1]. Developing and executing a PHIL simulation that is accurate, stable, and appropriately designed for a given hardware under test (HUT) can be challenging. In recent work [2], a common framework was developed with the goal of simplifying this process and providing a template upon which future test platforms can be designed to avoid duplicative effort. This framework modularizes the overall PHIL test platform into smaller application function blocks (AFBs), which can be individually reused and reconfigured based on the requirements of a given PHIL platform. Although the work in [2] introduced this valuable framework and demonstrates its utility, it did not directly address the important step of analyzing PHIL system stability before online operation. This paper aims to extend the work in [2] by developing a systematic approach to characterizing and analyzing a PHIL platform, as defined using the common framework of [2].

Some existing works use offline simulation and analytical study to evaluate the stability of the PHIL system. Quantitative studies of the stability and accuracy of PHIL test platforms assuming a grid impedance and HUT impedance were given in [3], [4]. Comprehensive analytical study was performed in [5], [6] to characterize the PHIL interface and investigate how key factors (e.g., interface noise and time delay) impact the stability of the PHIL platform. The authors of [7], [8] developed an interface compensation method and performed an analytical study to ensure the stability and accuracy of a PHIL platform. Similarly, a technique to improve PHIL system stability was developed in [9] by modifying the impedance ratio between the simulated system and HUT. Modeling and characterizing a PHIL power

amplifier to obtain the dynamic characteristic of the power interface for stability analysis was presented in [10].

This discussion reveals that existing work primarily focuses the stability assessments on the interface algorithm. In this work, however, a systematic stability evaluation of the entire PHIL platform is conducted to obtain a more complete stability assessment and to demonstrate how to apply the evaluation method to other PHIL platforms defined using the common framework of [2]. This end-to-end evaluation includes all software and hardware subsystems that form the closed loop of the PHIL experiment. Analyzing the entire closed loop ensures that the potential influences on the stability or accuracy of each individual component are taken into account and provides a complete model that can be used to design interfacing algorithms and controllers necessary for the PHIL system. The systematic stability assessment approach is demonstrated for a case study involving PHIL testing of a solar inverter and validated using experimental data. The remainder of this manuscript is organized as follows: the configuration of the overall PHIL platform is described in Section II. Systematic methods for characterizing the components of this platform and performing an end-to-end stability assessment of this platform are presented in Section III and Section IV, respectively. An experimental validation and demonstration are presented in Section V.

II. PHIL PLATFORM CONFIGURATION

An generalized electrical diagram of a PHIL platform for testing a grid-connected HUT is depicted in Fig. 1. The diagram includes the equivalent impedance of the simulated electrical power system (represented by Thevenin circuit V_s and Z_s), which will be executed on a digital real-time simulator (DRTS); the PHIL system software interface, including signal conditioning, interface algorithms, and system controllers; the PHIL system hardware interface, including analog/digital converters, power amplifier, and sensors; and the HUT. To facilitate the stability analysis of the PHIL platform shown in Fig. 1, a transfer function block diagram including all components in the PHIL system's closed loop is presented in Fig. 2 (seen also reference [7]). Blocks in this figure are grouped according to the AFB template presented in [2], though only AFB#2 (PHIL interfacing compensation, AFB#3 (analog output conditioning), and AFB#4 (analog input conditioning) are included in this stability analysis-focused diagram.

In Fig. 2, k_v is the scaling factor of the simulated voltage to the output voltage of the power amplifier. Similarly, k_I is the scaling factor for the measured current and is equal to the ratio of the power rating of the simulated HUT to the physical HUT (e.g., 50-kW physical HUT to 500-kW simulated HUT would have $k_I = 10$). G_{Reg} and G_{Comp} are the transfer functions of the voltage regulator and notch filter for interface

compensation, which are the elements of AFB#2 (PHIL interfacing compensation [7]). K_M , D_v , and K_I are the elements in AFB#3 (analog output conditioning); the meaning and value of each element can be found in [2]. G_{GS} is the voltage

output transfer function of the power amplifier, and Z_{GS} is the output impedance of the power amplifier, also known as a grid simulator (GS). G_{Txf} and H_{Txf} are the forward voltage ratio and backward current ratio of the transformer.

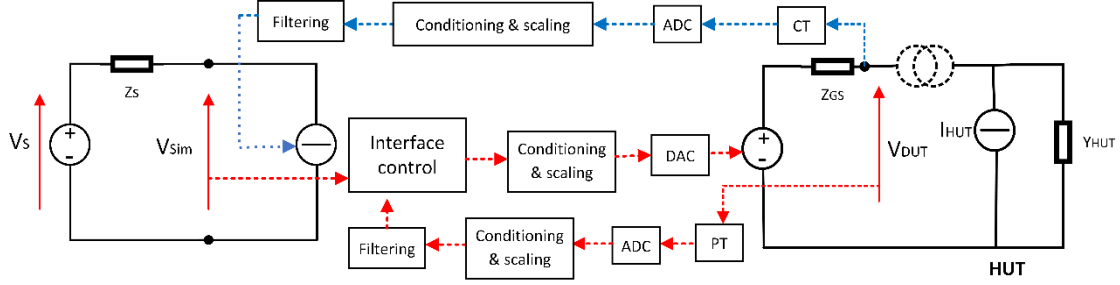


Fig. 1. Generalized electrical diagram of a PHIL experimental setup.

The HUT, a solar inverter for this case study, is represented by the inverter's parallel admittance, Y_{HUT} , and a current injection, I_{HUT} , which corresponds to the current reference for the HUT inverter. The elements of AFB#4 (analog input conditioning) are represented in the green box, including scaling and conditioning for both feedback current and voltage (see [2] for a further definition of each variable). H_{FBV} and H_{FBI} are voltage and current feedback filters. H_{PT} and H_{CT} are the transfer functions of the potential transducer (PT)

and current transducer (CT). K_{ADC} and K_{DAC} represent the analog-to-digital and digital-to-analog converters, respectively, in the DRTS I/O module. $H_{HWFilter}$ is an optional hardware filter installed in the analog input card of the DRTS to prevent aliasing. As shown in Fig. 2, all the elements in the PHIL system's closed loop are included to give a full representation of the PHIL simulation for stability evaluation. Characterization and determination of these values will be discussed in the following section.

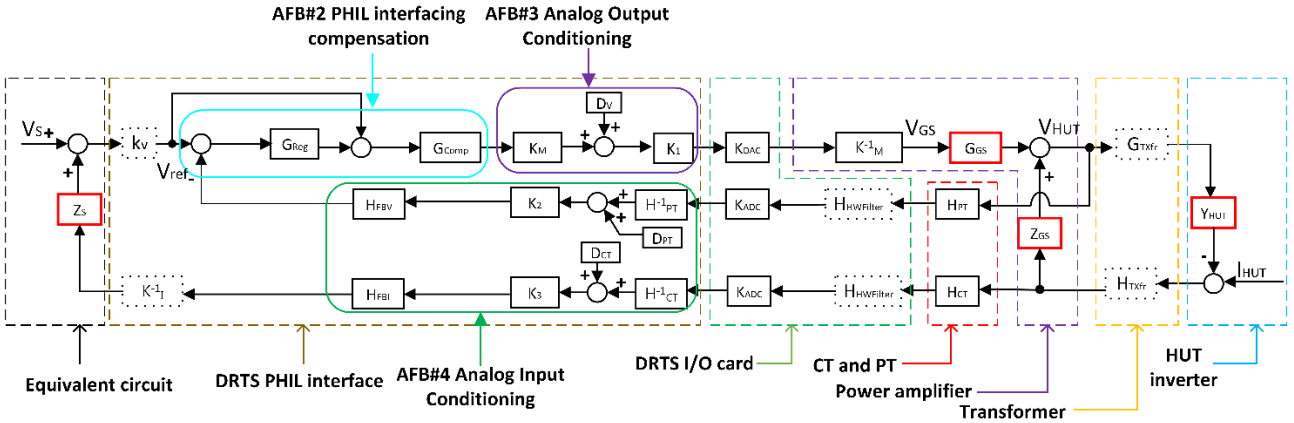


Fig. 2. Transfer function block diagram of the PHIL experimental setup including all the elements in the closed loop.

III. CHARACTERIZING THE PHIL PLATFORM

Before a comprehensive stability analysis can occur, the gains and transfer functions of Fig. 2 must be identified. Here, Z_s , G_{GS} , Z_{GS} , and Y_{HUT} are commonly determined by experimental tests/numerical simulation; G_{Reg} , G_{Comp} , H_{FBV} , and H_{FBI} needs to be designed by the user (in the paper we use approach in [7] for example design guidelines); and K_M , D_v , K_I , K_{DAC} , G_{Txf} , H_{Txf} , H_{PT} , H_{CT} , K_{ADC} , K_2 , K_3 , D_{PT} , D_{CT} , K_v , and K_I can be derived or estimated from element specifications/data sheet. In this section, the characterization of these elements is presented with a particular focus on the experimental determination of Z_s , G_{GS} , Z_{GS} , and Y_{HUT} .

A. Virtual System Equivalent Grid Impedance Z_s

The equivalent impedance (Z_s) of the simulated power system model seen at the point of common coupling (PCC) of the HUT can be obtained via a frequency scan within the simulated power system model, a technique commonly used in studying the stability of the grid-connected inverters where

knowledge of the grid impedance value is important. As shown in Fig. 1, this impedance is the impedance of the Thevenin equivalent circuit, where the controlled-current source representing the HUT is connected in the real-time simulated power system model. A frequency scan is completed by connecting a sinusoidal voltage source behind a small resistance at the PCC in the simulated model where the HUT will be connected and then measuring the resulting simulated current [11]. By using both the voltage and current signals measured at the PCC, we can obtain both the magnitude and phase of the circuit impedance for that particular frequency. Note that all other generation units should be removed from the simulated power system model to create a purely passive circuit network.

A schematic diagram is shown in Fig. 3 to illustrate how to implement the frequency scan to calculate the grid impedance Z_s ($Z_s = Z_{Re} + jZ_{Im}$). A very small resistance (as small as possible, e.g., $1e-4 \Omega$) is connected in series with the injected voltage source, which is controlled by the generated

three-phase voltage (V_a, V_b, V_c) with the phase angle named “Phase.” The magnitude of the three-phase voltage source (“Magnitude”) should be in the same as the magnitude of the voltage for the circuit under test. For example, for a simulated distribution power system model with nominal 480-V line-to-line bus voltage, a line-neutral voltage reference of 391 V was used in the frequency scan. The frequency (“Freq”) is an adjustable value that has a minimum and maximum limit and step size to contain the frequency range of interest. In this example, a range of 1–80 Hz with a step size of 1 Hz was used for nominal frequency of 60 Hz. The measured voltage at the terminal of the testing circuit v and the measured current i are processed through discrete Fourier transformation (DFT) with the same angle “Phase” and converted to complex variables. Then, the complex voltage is divided by the complex current, and the real (Z_{Re}) and imaginary (Z_{Im}) part of the grid impedance is obtained after converting from complex variables.

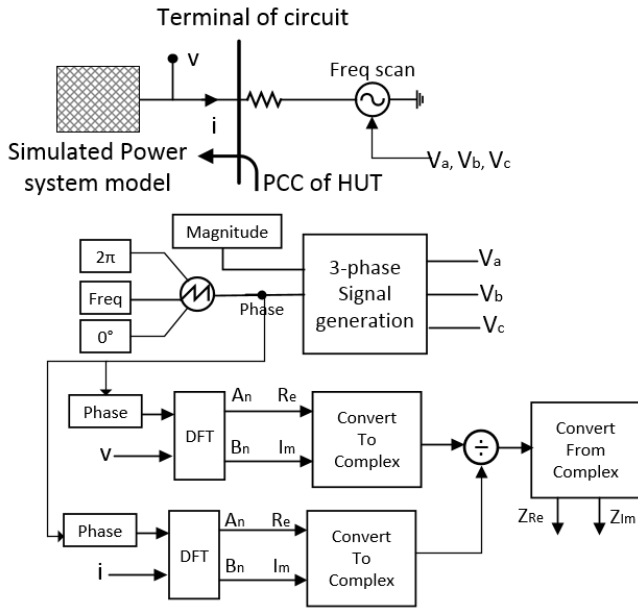


Fig. 3. Schematic diagram of the frequency scan to calculate the equivalent grid impedance from the simulated power system model [11].

Applying the frequency scan approach in the selected electric grid, the output impedance we obtain is $Z_s = 0.055 + j0.12$ with $R_s = 0.055 \Omega$ and $L_s = 100.2 \mu H$.

B. Power Amplifier G_{GS} and Z_{GS}

Power amplifiers used for PHIL are commonly voltage source amplifiers that amplify a target AC voltage (e.g., v_{in}) from the DRTS simulation model to an output voltage (e.g., v_{out}) at the full-scale voltage level of the HUT. For the case study considered, the power amplifier was a back-to-back switch mode power supply (see Fig. 4(a)) wherein a cascaded voltage regulator controls (VC: voltage controller, CC: current controller) the converter’s switches via pulse-width modulation to regulate the output voltage v_{out} of the HUT (see Fig. 4(b)). The closed-loop transfer function of the power amplifier can be expressed as $v_{out}(s) = G_{GS}v_{in}(s) - Z_{GS}(s)i_{out}(s)$ [6], and the equivalent circuit is shown in Fig. 4(c). Here, G_{GS} is the amplifier gain, Z_{GS} is the output impedance, $v_{in}(s)$ is the voltage reference, $v_{out}(s)$ is the output voltage, and $i_{out}(s)$ is the output current. $G_{GS}(s)$ and $Z_{GS}(s)$ are the key parameters to be determined to characterize the dynamics of a power amplifier. These two parameters are

intrinsic to the power amplifier and can be considered independent of the testing conditions (sink/source mode, reference voltage, power level) when holding the common assumption of timescale separation from the switching timescale dynamics. Methods for determining these key parameters are presented next.

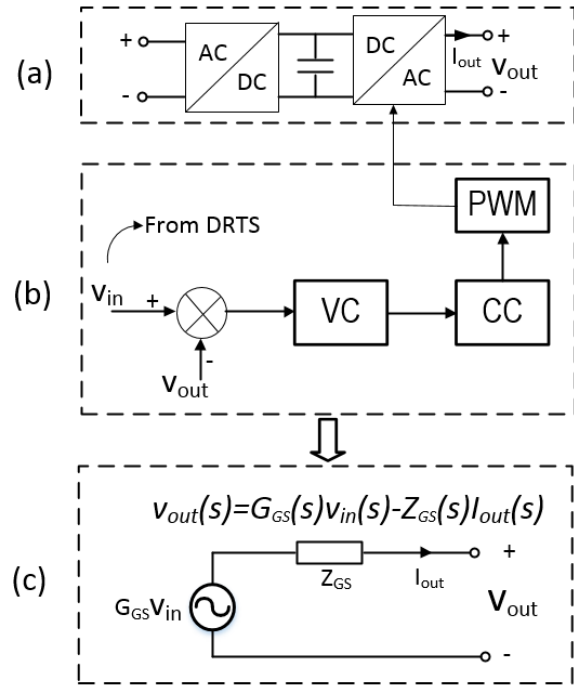


Fig. 4. Representation of the power amplifier (a) physical circuit, (b) control diagram, and (c) equivalent circuit.

(1) Determine the amplifier gain $G_{GS}(s)$

In order to determine the amplifier gain, the power amplifier is analyzed under no load conditions, when $i_{out}(s) = 0$, so the amplifier gain is $G_{GS} = V_{out}(s)/V_{in}(s)$. Thus, the amplifier gain G_{GS} can be identified for a known V_{in} and V_{out} pair, and when considering many $\frac{V_{out}(j\omega)}{V_{in}(j\omega)}$ pairs at differing frequencies, a frequency response $G_{GS}(j\omega)$ and transfer function $G_{GS}(s)$ can be estimated. Here, this approach is implemented by conducting frequency sweep experiments using the experimental setup shown in Fig. 5; the reference voltage is set to $V_{in}(j\omega) = V_{in,0}(j\omega_0) + V_{in,k}(j\omega_k)$, where $V_{in,0}(j\omega_0)$ is a fundamental frequency component ($\omega_0 = 2\pi \cdot 60$ rad/s here), and $V_{in,k}(j\omega_k)$ is a harmonic component at frequency $\omega_k = k \cdot \omega_0$. Throughout, $|V_{in,0}(j\omega)| = 1.0$ p.u. as the power amplifier, which will operate around the HUT rated voltage while testing; and $|V_{in,k}(j\omega_k)| = \{0.05, 0.1\}$ p.u. (two different test cases are considered), which injects a relatively small-magnitude frequency component. This is repeated for $k = 3, 5, \dots, 49$, and each point is held for 5 seconds, during which the time-domain voltage reference, $V_{in}(t)$, and measured output voltage of the power amplifier, $V_{out}(t)$, are simultaneously sampled at $F_s = 50$ kHz by a high-bandwidth oscilloscope with appropriate voltage probes. Fourier transform techniques can be used to obtain $V_{out}(j\omega)$ and $V_{in}(j\omega)$ and ultimately the power amplifier frequency response $G_{GS}(j\omega)$.

An alternate approach to obtain the transfer function model $G_{GS}(s)$ from the same measured, $V_{in}(t)$ and $V_{out}(t)$, data is to apply system identification techniques to fit a model. This approach was found to generate more accurate results but

relies on knowledge of a prototype transfer function model. Based on experience from an internal project and as summarized in [10], the response of a switch mode power supply amplifier can be represented by a first-order transfer function or a third-order transfer function. Because the error between the first-order model and the third-order model can be very small, the first-order transfer function is used for simplicity:

$$G_{GS}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G}{s+P_0} e^{-sT_{delay}} \quad (1)$$

where T_{delay} is the estimated time delay and is approximated as one time step of the real-time simulation (here, $T_{delay} = 30 \mu s$). A grey box system identification approach is then applied using the MATLAB system identification toolbox, with $V_{in}(t)$ as the model input; $V_{out}(t)$ as the model output; (1) as the grey box model; and G and P_0 as the parameters to be estimated.

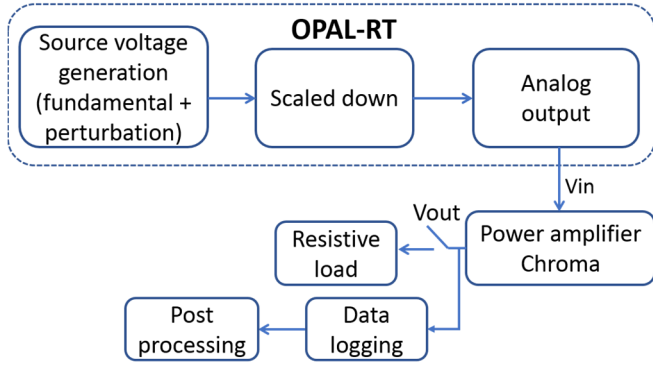


Fig. 5. Diagram of experimental setup used for characterizing the power amplifier.

The obtained results using the alternate approach are shown in Fig. 6. The blue line represents the model transfer function estimated when using $V_{in,k}(j\omega_k) = 0.05$ p.u., and the red line represents the case for $V_{in,k}(j\omega_k) = 0.1$ p.u. These two transfer functions have good accuracy, with errors less than 1% in both magnitude and phase angle. The transfer function with less error (10% harmonics) is selected. Thus, the obtained transfer function of the amplifier gain G_{GS} is $G_{GS}(s) = \frac{4.6427e3}{s+4.6814e3} e^{-s0.00003}$. The phase shift at 60 Hz is -4.6 degree, and the cutoff frequency is 800 Hz.

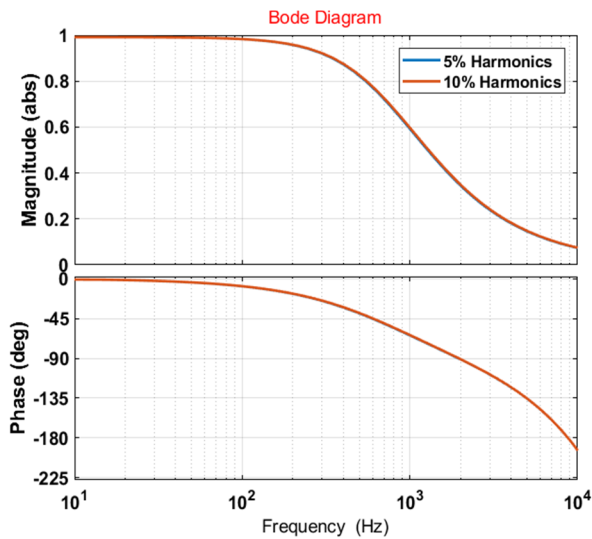


Fig. 6. Bode diagram showing the frequency response of the amplifier gain $G_{GS}(s)$.

(2) Determine the output impedance Z_{GS}

There are three methods to determine the output impedance Z_{GS} :

(i) If the electrical schematic diagram and the parameters of the ac output filter are available, it is possible to calculate Z_{GS} directly.

(ii) If the condition in (i) does not apply, it might be possible to open the enclosure of the de-energized power amplifier and measure the discrete values of the ac output filter directly using an LCR meter.

(iii) Perform experiments to determine the output impedance of the power amplifier using the experimental setup shown in Fig. 5, with the resistive load (Z_{load}) connected. Fig. 4(c) shows that the representation of the output impedance Z_{GS} can be expressed as:

$$Z_{GS}(s) = \frac{G_{GS}(s)V_{in}(s) - V_{out}(s)}{V_{out}(s)/Z_{load}(s)} = (G_{GS}(s) \frac{V_{in}(s)}{V_{out}(s)} - 1)Z_{load}(s) \quad (2)$$

As with identification of the amplifier gain, a frequency sweep test, conducted under different loading conditions (0.25, 0.5, 0.75, and 1 p.u.), followed by grey box system identification, can be used to identify $Z_{GS}(s)$.

Here, the second approach (ii) is taken. The ac output filter was found to be of LCL topology with measured parameters: $L_1 = 97 \mu H$, $C = 17.5 \mu F$, and $L_2 = 3.7 mH$. The circuit for single phase is shown in Fig. 7.

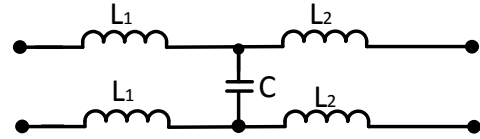


Fig. 7. Output filter of the grid simulator.

The calculated output impedance is then:

$$Z_{GS}(s) = 7.4e^{-3}s + \frac{1}{197e^{-6}17.5e^{-6}s^2 + 1} \quad (3)$$

The bode plot of the output impedance $Z_{GS}(s)$ is shown in Fig. 8.

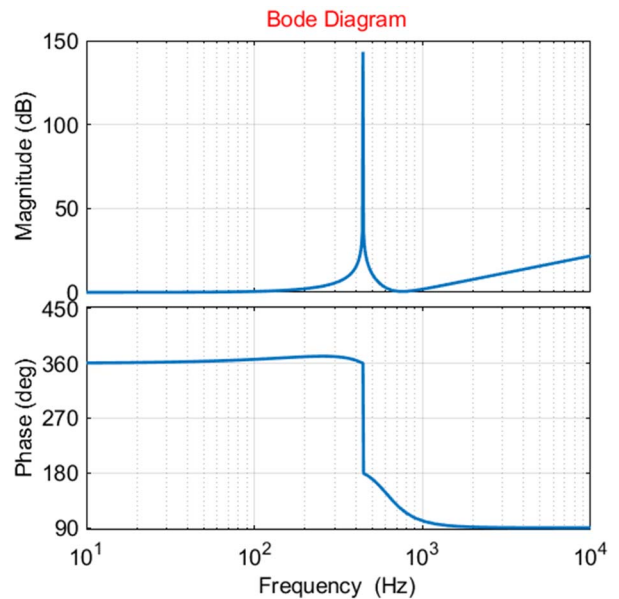


Fig. 8. Bode plot of the output impedance of grid simulator, $Z_{GS}(s)$.

C. Hardware Under Test Inverter Y_{HUT}

The HUT inverter is modeled as a Norton equivalent comprising a controlled-current source I_{HUT} with a parallel-connected admittance Y_{HUT} . Assuming that the inverter has an LC filter, a circuit diagram of the HUT inverter with LC filter connected at the grid side and the equivalent Norton circuit is shown in Fig. 9.

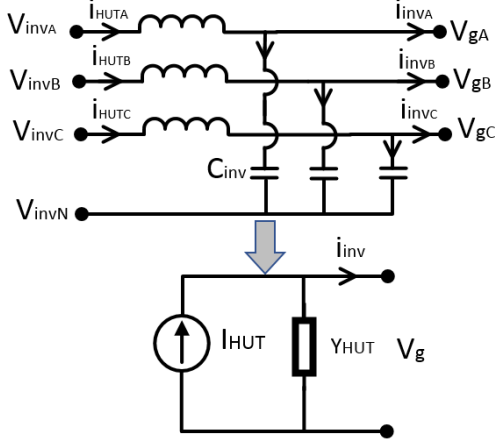


Fig. 9. Circuit diagram of HUT inverter.

To calculate the equivalent admittance, we need to derive the relationship between i_{inv} and i_{HUT} , where i_{inv} is the output current of the inverter flowing to the grid, and i_{HUT} is the output current before the LC filter. Assuming balanced operation, the following equations hold:

$$i_{invA} = i_{HUTA} - \frac{V_{gA} - V_{invN}}{1/sC_{inv}} \quad (4)$$

$$\frac{V_{gA} - V_{invN}}{1/sC_{inv}} + \frac{V_{gB} - V_{invN}}{1/sC_{inv}} + \frac{V_{gC} - V_{invN}}{1/sC_{inv}} = 0 \quad (5)$$

where V_{inv} is the inverter voltage before the LC filter, V_g is the output voltage, C_{inv} is the capacitor of the LC filter, and V_{invN} is the neutral voltage of the inverter. Substituting (5) into (4), (6) is obtained as:

$$i_{invA} = i_{HUTA} - \frac{2}{3}V_{gA}sC_{inv} + \frac{1}{3}(V_{gB} + V_{gC})sC_{inv} \quad (6)$$

Extending (6) for the full three-phase system, the following equations showing the relationship between i_{inv} and i_{HUT} are obtained:

$$\begin{bmatrix} \dot{i}_{invA} \\ \dot{i}_{invB} \\ \dot{i}_{invC} \end{bmatrix} = \begin{bmatrix} \dot{i}_{HUTA} \\ \dot{i}_{HUTB} \\ \dot{i}_{HUTC} \end{bmatrix} - sC_{inv} \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \quad (7)$$

Therefore, we obtain:

$$Y_{HUT} = C_{inv} \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \quad (8)$$

Ignoring the cross-coupling components between phases, we get the equivalent admittance for each phase as:

$$Y_{HUT} = \frac{2}{3}sC_{inv} \quad (9)$$

IV. SYSTEM STABILITY EVALUATION

An advantage of the comprehensive PHIL system analysis approach presented in this work is that all components and transfer functions in the system's closed loop are fully considered; this allows for comprehensive stability analysis as well as more robust control design. In this work, a stability analysis using the closed-loop transfer function is presented and then compared to a more commonly used open-loop transfer function-based analysis. To derive the closed-loop function of the entire PHIL simulation shown in Fig. 2, we define $H_{VF} = H_{PT}K_{ADC}H_{PT}^{-1}H_{FBV}$ and $H_{IF} = H_{CT}K_{ADC}H_{CT}^{-1}H_{FBI}$. A few intermediate steps are derived and shown in (10)–(12):

$$G_{V_{HUT}, V_{GS}} = \frac{V_{DUT}}{V_{GS}} = \frac{1}{1+Z_{GS}Y_{HUT}} \quad (10)$$

$$G_1 = \frac{V_{HUT}}{V_{ref}} = \frac{(1+G_{Reg})G_{Comp}K_{DAC}G_{GS}}{H_{VF}G_{Reg}G_{Comp}K_{DAC}G_{GS}+1+Z_{GS}Y_{HUT}} \quad (11)$$

$$V_s + H_{IF}Z_S I_{HUT} = \left(\frac{1}{G_1} + Y_{HUT}H_{IF}Z_S\right)V_{DUT} \quad (12)$$

Substituting (11) into (12), the full representation of the closed-loop transfer function is obtained as:

$$V_{HUT} = \frac{G_1}{1+Y_{HUT}H_{IF}Z_S G_1} V_s + \frac{G_1 H_{IF} Z_S}{1+Y_{HUT}H_{IF}Z_S G_1} I_{HUT} \quad (13)$$

Based on the calculation and characterization in Section III, the transfer function of each component in (13) is listed in Table II. As shown by (13), the PHIL simulation is a two-input and one-output system, with the control input being the voltage of the equivalent voltage source, V_s , and the disturbance input being the output current of the HUT, I_{HUT} . To verify stability, the two transfer functions $\frac{V_{HUT}}{V_s}$ and $\frac{V_{HUT}}{I_{HUT}}$ need to be evaluated. As shown by (13), the denominators of these two gains are identical, so only the stability of transfer function $\frac{V_{HUT}}{V_s}$ is evaluated.

One common method of analyzing PHIL system stability, especially when the ideal transformer method (ITM) interface algorithm is used (as it is in this study), is to consider the magnitude of the impedance ratio (Z_s/Z_{HUT}) and the total time delay and then determine stability by applying the Nyquist criteria on the open-loop transfer function [5]. Based on the closed-loop transfer function in (13), the open-loop transfer function can be obtained as: $G_{OL}(s) = Y_{HUT}H_{IF}Z_S G_1 = \frac{Y_{HUT}H_{IF}Z_S(1+G_{Reg})G_{Comp}K_{DAC}G_{GS}}{1+H_{VF}G_{Reg}G_{Comp}K_{DAC}G_{GS}+Z_{GS}Y_{HUT}}$ (14)

Substituting the values listed in Table II into (14), a numerical representation of the open-loop transfer function and a resulting Nyquist plot are obtained as shown in Fig. 10. As shown, the critical point (-1, 0) is not encircled by the curve. Thus, the system is stable. The gain margin is 3.83 dB and the phase margin is 35.8°, indicating that the system still has some stability margin. The stability analysis of the closed-loop transfer function is presented next. The stability and accuracy of the case study system is demonstrated by experimental test.

The eigenvalues of the closed-loop transfer function shown in (13) are calculated to evaluate the closed-loop stability. The pole-zero map is shown in Fig. 11, and the specific pole values are given in Table I. All the poles of this 21st-order system are in the strict left-half s-plane, validating that the closed-loop HIL platform is stable. To give better resolution, the poles are listed in Table 1.

TABLE I. LIST OF POLES OF THE CLOSED-LOOP PHIL SYSTEM

-4e4	-4e4	-0.4681e4
-3 + 377j	-3 - 377j	-4e4
-4e4	-4.3043e4	-3.6587e4
-109 + 3.0537e4j	-109 - 3.0537e4j	-0.5088e4
-0.4681e4	-0.151e4	-0.08e4
-0.08e4	-7 + 0.0677e4j	-7 - 0.0677e4j
-3 + 0.0377e4j	-3 - 0.0377e4j	-117

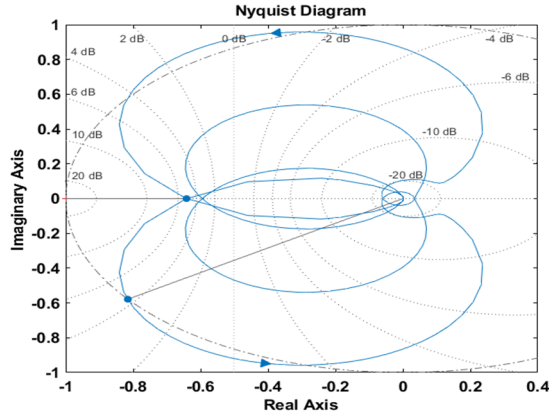


Fig. 10. Nyquist diagram of the open-loop transfer function $G_{OL}(s)$.

An additional important insight from the stability analysis is that even though the ITM interface is used, the stability analysis cannot simply be evaluated based on the impedance

ratio (Z_s/Z_{HUT}) and the simplified open-loop transfer function shown in [4]. The additional elements (e.g., G_{Reg} and G_{Comp}) are added into the PHIL loop, which changes the characteristic of the whole system. The traditional open-loop ITM stability analysis method may concur with the results of the closed-loop analysis method, but it is not a sufficient method to guarantee closed-loop stability. Thus, it is necessary to derive the complete open- and closed-loop transfer function, as we do in this paper.

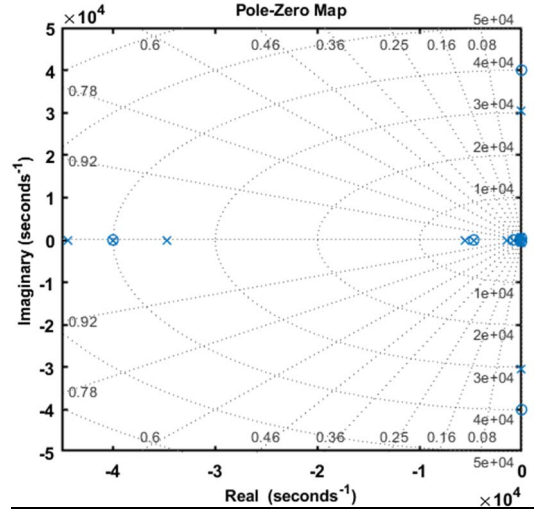


Fig. 11. Pole-zero map of the closed-loop transfer function $G_{CL}(s)$.

TABLE II. LIST OF ELEMENTS CHARACTERIZING THE PHIL EXPERIMENTAL SETUP

Element	Description	Expression	Values
G_{Reg}	Voltage regulator to tracking the fundamental frequency 60 Hz	$\frac{2K_r \omega_c s}{s^2 + 2\omega_c s + \omega_0^2}$	$K_r = 150, \omega_c = 2\pi \cdot 0.5, \omega_0 = 2\pi \cdot 60$
G_{comp}	Notch filter to eliminate the resonance in the current loop	$\frac{s^2 + \omega_n^2}{(s + \omega_n)^2}$	ω_n is equal to the parasitic resonance frequency [7]
K_{ADC}	Transfer function of the ADC	1 step delay $e^{-sT_{DRTS}}$	$T_{DRTS} = 50\mu s$
K_{DAC}	Transfer function of the DAC	1 step delay $e^{-sT_{DRTS}}$	$T_{DRTS} = 50\mu s$
G_{GS}	Amplifier gain of the power amplifier	$\frac{G}{s + P_0} e^{-sT_{GS}}$	$G = 4.6427e3, T_{GS} = 30e-6$ $P_0 = 4.6814e3$
$H_{FB,V}$	Voltage feedback filtering using a second-order lower pass filter	$\left(\frac{\omega_{FBV}}{s + \omega_{FBV}}\right)^2$	$\omega_{FBV} = 2\pi \cdot 800$ rad/sec
Z_{GS}	The output impedance of the power amplifier	$R_{GS} + j\omega L_{GS}$	$R_{GS} = 10m\Omega, L_{GS} = 3.8mH$
Y_{Inv}	The HUT inverter admittance	$\frac{2}{3} s C_{Inv}$	$C_{Inv} = 40\mu F$
$H_{FB,I}$	Current feedback filtering using a second-order lower pass filter	$\left(\frac{\omega_{FBI}}{s + \omega_{FBI}}\right)^2$	$\omega_{FBI} = 2\pi \cdot 800$ rad/sec
Z_s	Equivalent impedance of the network seen by the PCC at fundamental frequency	$R_s + j\omega L_s$	$R_s = 50.5m\Omega$ $L_s = 100.2\mu H$

V. EXPERIMENTAL RESULTS

Experimental tests are performed to further demonstrate the stability of the example PHIL setup analyzed during the course of this work. The platform which was characterized in the previous section is shown in Fig. 12. A 12-kVA PV inverter is the HUT and is connected to a simple distribution system, modeled in real time on an OPAL-RT real-time

simulator. A 60-kVA power amplifier along with CTs and PTs are used to interface the HUT to the real-time model. The HUT is operated at different power levels to verify system stability under a variety of operating conditions with unity power factor. A PV-array emulator is used to provide the power at the DC input of the PV inverter. Because the PV inverter is producing power, the grid simulator works in power sink mode. To limit noise and EMI interference, the current

transducer, potential transducer, and their analog connections to the DRTS are shielded. For safety, the test procedures outlined in [10] are followed.

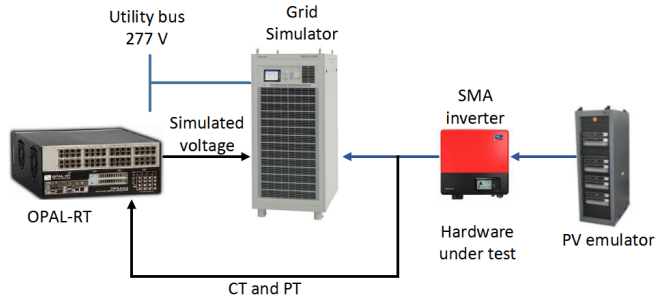


Fig. 12. Example PHIL setup for stability validation

Summary results from operating the HUT at six different power levels across its range of operation are shown in Table III. Operation under all power levels is stable, as expected from the previous analytical stability analysis. With an improperly interfaced PHIL experiment, there is potential for mismatch between the measured power at the HUT and the power injected back into the real-time power system model; however, after compensating the PHIL experiment using the steps described in earlier sections, this interfacing provided good accuracy within 2.5% (comparing the injected active power in the DRTS model with the active power measured at the terminals of the power amplifier where the HUT was connected). Note that the delay in feedback current caused the controlled-current source to consume reactive power. This results in the deviation in reactive power. Because the values of the reactive power (in power amplifier and the injected source in DRTS) are so small, the calculated error in reactive power (%) is large; however, the amount is less than 210 Var, which is acceptable for this experiment. Therefore, the preliminary experimental tests shown here further demonstrate the stability of the PHIL platform with the chosen interface algorithm and HIL setup.

TABLE III. LIST OF MEASUREMENT RESULTS

Power Amplifier Measured Power		DRTS Injected Power		Accuracy
Active power (kW)	Reactive power (kVar)	Active power (kW)	Reactive power (kVar)	Error in active power (%)
2.36	0.1	2.315	-0.173	-1.91
3.9	0.07	3.812	-0.175	-2.26
5.97	0.32	5.851	-0.186	-1.99
8.04	0.34	7.868	-0.192	-2.14
10.102	0.34	9.869	-0.195	-2.31
11.85	0.34	11.6	-0.207	-2.11

Detailed results of the HUT operating at 6 kW are presented in Fig. 13–Fig. 15 and further demonstrate the stability and accuracy of the PHIL simulation platform. Fig. 13 shows the voltage-tracking capability of the PHIL platform without (before $t = 275.33$ s) and with the platform’s voltage regulator turned on by comparing the voltage reference from the real-time power system model (blue trace) with the measured voltage at the output of the grid simulator (red trace). It is clear that these voltages match much more closely after turning on the voltage regulator, demonstrating the important role of a voltage regulator in a PHIL test setup. The error between the reference voltage and the measured voltage

for each phase when turning on the voltage regulator is shown in Fig. 14. The magnitude of the voltage error before turning on the voltage regulator is about 80 V, which is large because of the phase delay and magnitude deviation between the reference voltage and the measured feedback voltage from PT. The output active and reactive power of the HUT is also shown in Fig. 15, which shows improved accuracy after turning on the voltage regulator.

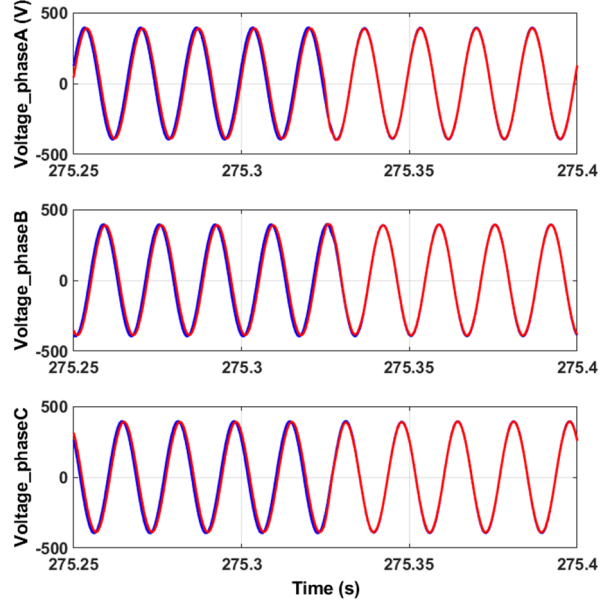


Fig. 13. Closed-loop test of turning on the voltage regulator.

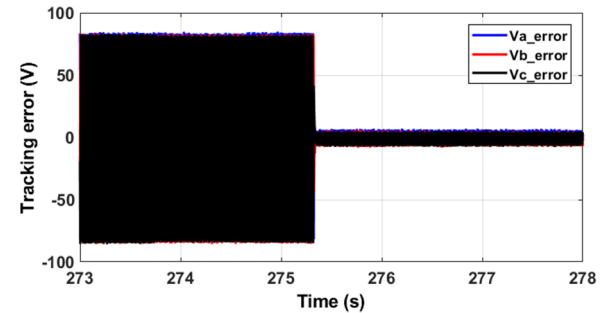


Fig. 14. Closed-loop test of tracking error turning on voltage regulator.

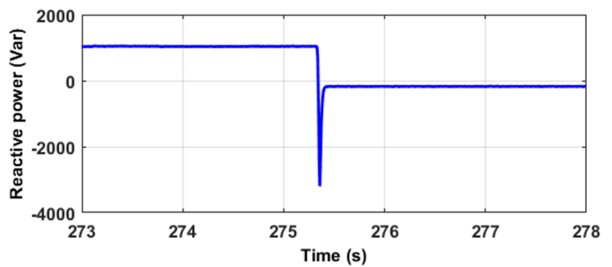
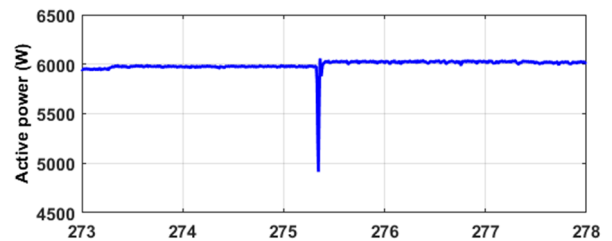


Fig. 15. Closed-loop test of active and reactive power of PV inverter in OPAL-RT.

VI. CONCLUSION

This paper presents the stability evaluation of a PHIL platform prior to normal lab test and study. First, a diagram of the PHIL platform including all the associated elements are presented to give a high-level view of the system. Then, characterization is performed to get the mathematical representation of each element with special focus on four elements: amplifier gain and output impedance of the power amplifier, equivalent voltage source impedance, and equivalent HUT admittance. Next, the stability is evaluated analytically by checking the open-loop transfer function by the Nyquist Criteria and poles of the closed-loop system. Even though the ITM interface approach is used, it is necessary to perform both open-loop and closed-loop analysis. The analytical result provides preliminary stability evaluation of the PHIL simulation system. In the end, experimental tests are performed to further demonstrate the stability of the PHIL system. This work provides a highly efficient tool to predict the stability of the PHIL simulation beforehand with accurate models of the components in the loop.

ACKNOWLEDGMENT

This work was supported by Alliance for Sustainable Energy, LLC, the manager and operator of the National Renewable Energy Laboratory for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding provided by U.S. Department of Energy Office of Electricity, Advanced Grid Research & Development. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide

license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

REFERENCES

- [1] R. Bruendlinger, et al., "Lab Test: Verifying That Smart Grid Power Converters Are Truly Smart," *IEEE Power & Energy Magazine*, pp. 31-43, March 2015.
- [2] J. Wang, et al., "Development of Application Function Blocks for Power-Hardware-in-the-Loop Testing of Grid-connected Inverters," 2019 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 1-8, June, 2018.
- [3] G. F. Lauss, M. Faruque, K. Schoder, C. Dufour, A. Viehweider and J. Langston, "Characteristics and Design of Power Hardware-in-the-Loop Simulations for Electrical Power Systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 406-417, Jan. 2016.
- [4] Z. Zhang and L. Flickert, "Power Hardware-in-the-Loop Testing for the Inverter-based Distributed Power Source," Symposium Energieinnovation, Graz, Austria, 2016.
- [5] Z. Zhang, L. Flicert and Y. Zhang, "Power Hardware-in-the-loop Test for Cyber Physical Renewable Energy Infeed," 2016 17th International Scientific Conference on Electric Power Engineering (EPE), pp. 1-6, 2016.
- [6] RTDS, "Power Hardware In The Loop Simulation", available: https://www.rtds.com/wp-content/uploads/2015/12/RTDS_PHIL_Report-1.pdf.
- [7] N. Ainsworth, et al., "Modeling and Compensation Design for a Power Hardware-in-the-Loop Simulation of an AC Distribution System," 2016 North American Power Symposium (NAPS), Denver, CO, 2016, pp.1-6.
- [8] K. Luo, et al., "Stability and Accuracy Considerations in the Design and Implementation of Wind Turbine Power Hardware in the Loop Platform," *Journal of Power and Energy System*, vol. 3, no. 2, pp. 167-175, June 2017.
- [9] X. Zha, et al., "Improving the Stability and Accuracy of Power Hardware-in-the-Loop Simulation Using Virtual Impedance Method," *Energise*, 2016, 9, 974, pp. 1-16.
- [10] K. Schoder, 3rd Annual International Workshop on Grid Simulator Testing Topic: "Modeling and Characterizing a Power Hardware-in-the-Loop Amplifier," The Center for Advanced Power Systems, Tallahassee, FL, November 5, 2015.
- [11] Harmonic Impedance Scan Sample Case. RTDS tutorial.