
OPAL-RT
TECHNOLOGIES
RT18
BUILDING
THE FUTURE
Power Electronic Control over the Network
RT18, Paris, France
November 14-16, 2018
J. Van den Keybus, CEO
triphase

Introduction

- Two presentations on Power Hardware In the Loop (PHIL) systems
  - Switch-mode power stages or modules
- Data network infrastructure (1:30 PM – 2:00 PM)
  - Essential for connection of many power electronics modules or components
- Modeling for improved performance (3:00 PM – 3:30 PM)
  - Mitigate or alleviate the single perceived weakness of switch-mode stage based PHIL systems

Power Electronics Control over the Network

- Customers often ask
  - Why the custom network protocol ?
  - Why multiple physical interfaces ?
- Development of many years
  - Part of company vision:

> Creating complex power conversion systems should be as simple as connecting power electronic building blocks to a network with a secure central computing platform for ease of use, quick development and optimal performance.

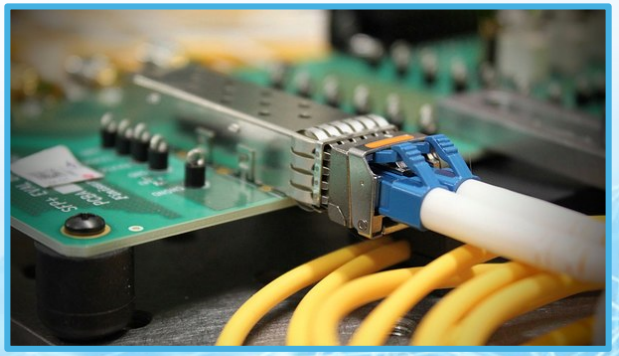
  - 10 years of 100 Mb/s and 1 Gb/s Ethernet → no longer used
- Most important reasons: cost, reliability and safety
- Importance underestimated
  - growing number of interconnected systems
  - significant amounts of electrical interference

Example system

- 8-channel, 3 ph. 400 V, 225 kW PHIL system
  - Channel: 12 SiC modules, 112 kHz, 400 V, 24 A, 3 ph. input and output
  - Local / central control: 112 kHz update rate, 0+ / 1 cycle latency

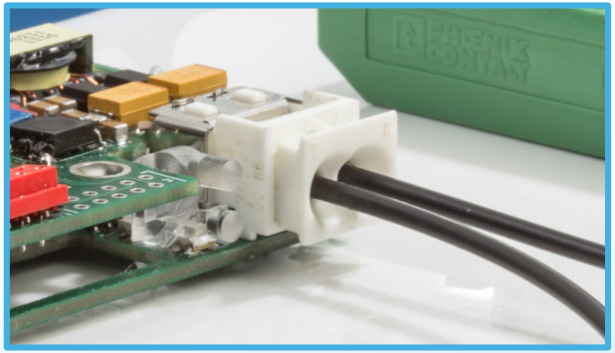
Physical interface / link cost

- 4 Gb/s SFP (Multi-Mode Fiber – MMF)
  - SFP module: 35 €, cable: 5 €
  - Mature, cost optimized → unlikely to become much cheaper
  - Additional ASIC / FPGA cost for SERDES transceiver
    - Intel / Altera EP4CE22F17C8N (Cyclone IV, 22k LE): 39 €
    - Intel / Altera 5CGTFD5C5F23C7N (Cycle V, 77k LE): 144 €
  - Additional PCB tech. (6 or 8 layers) and area (SFP cage) cost: 10 €
- Total cost: 102 €
  - 50% FPGA MSRP



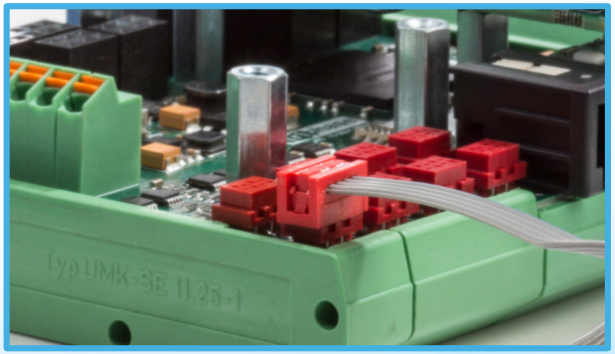
Physical interface / link cost

- 250 Mb/s POF (Plastic Optical Fiber)
  - Transceiver module: 15 €, cable: 1 €
  - In full development, driven by automotive → likely to become cheaper
- Total cost: 16 €



Physical interface / link cost

- 16 Mb/s Cu (Flat cable)
  - Transceiver: 1.5 €, cable: 0.3 €
  - Simplified data recovery in ASIC / FPGA
  - Also carries power supply for lower cost
- Total cost: 1.8 €



Required network bandwidth

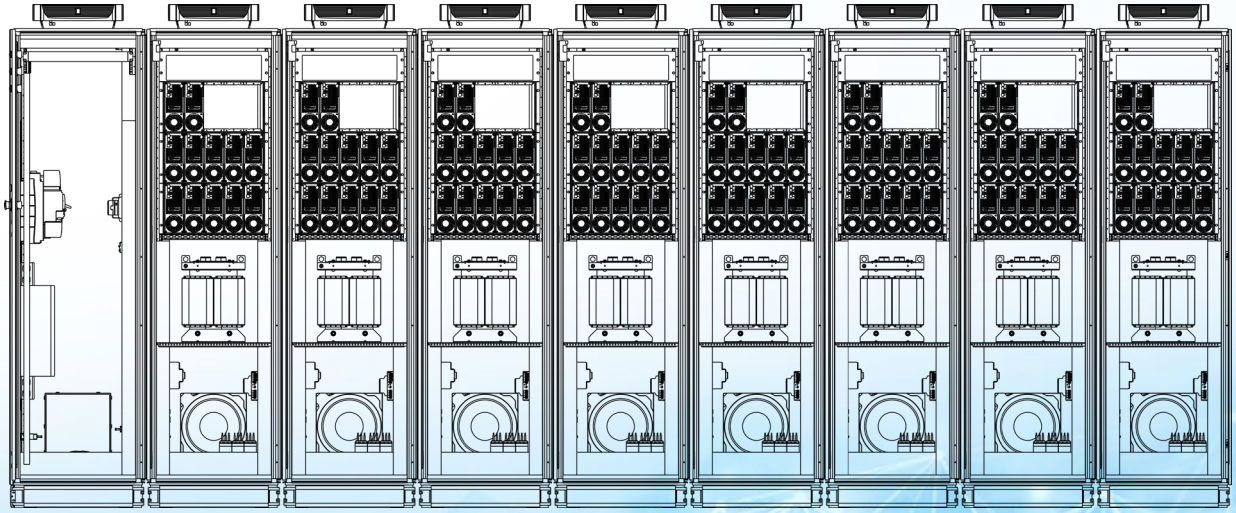
- Minimum data rates:
  - Module: 12.54 Mb/s
    - 112 kHz rate
    - RX: 6 bytes (ref. values), TX: 8 bytes (meas. values)
  - Cabinet: 150 Mb/s
  - System: 1.20 Gb/s
- Required link bandwidth
  - 30% link bandwidth utilization
  - 2 groups of 6 modules in 2 250 Mb/s POF rings per cabinet (16 rings total)
- Calculate cost for 3 architectures

Cost analysis

- 8 cabinets for 96 PMSiC modules, transformer, contactors
- 1 cabinet for central controller

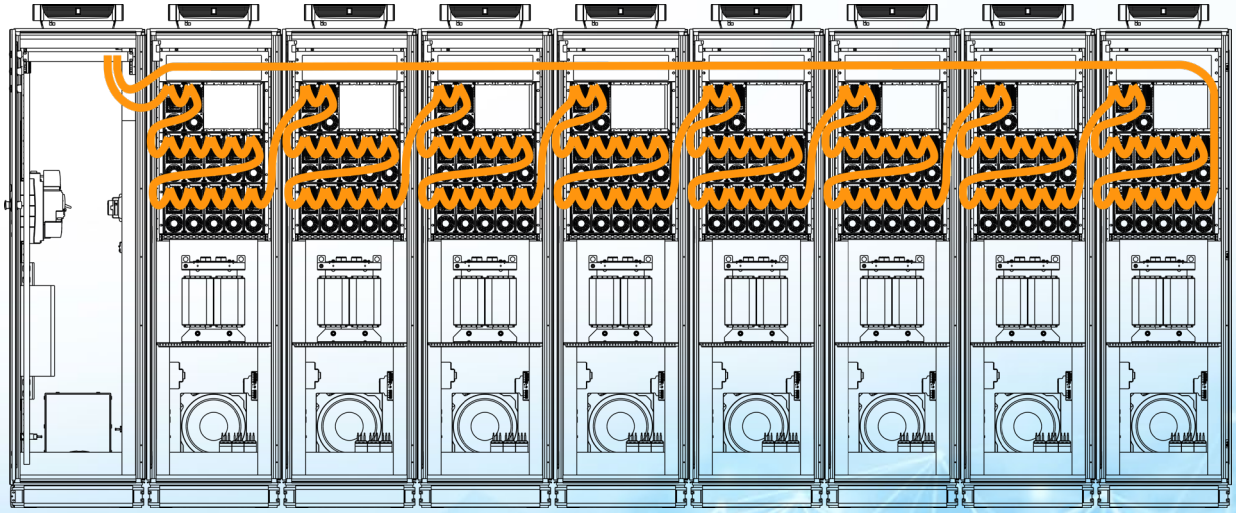
Cost analysis

- 8 cabinets for 96 PMSiC modules, transformer, contactors
- 1 cabinet for central controller



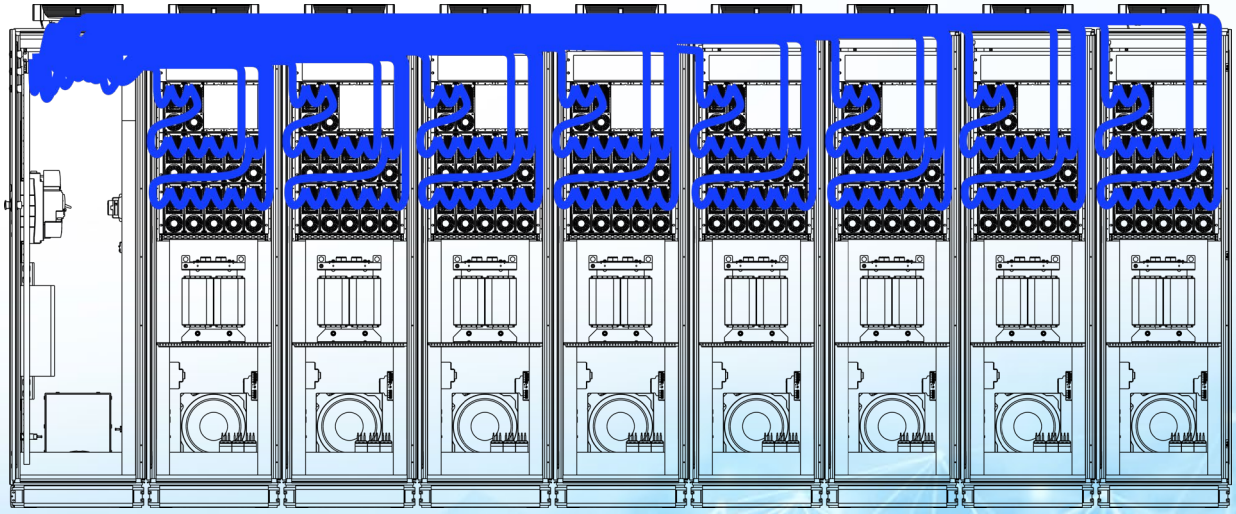
Cost analysis: network architecture 1

- Links: 97x 4 Gb/s MMF
- Total link cost: 9,894 €



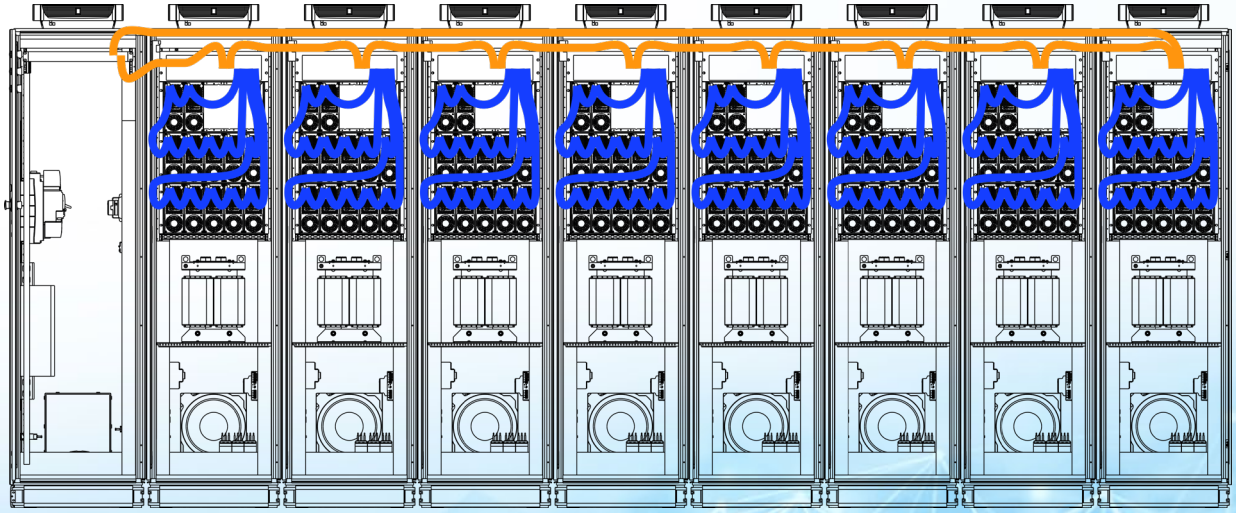
Cost analysis: network architecture 2

- Links: 112x 250Mb/s POF
- Total link cost: 1,792 €
- Significant disadvantages: cable mess, multiple PCIe cards



Cost analysis: network architecture 3

- Links: 9x 4 Gb/s MMF, 112x 250 Mb/s POF
- Switches: 8x 1 MMF port, 2 POF ports
- Total link cost: 2,710 €

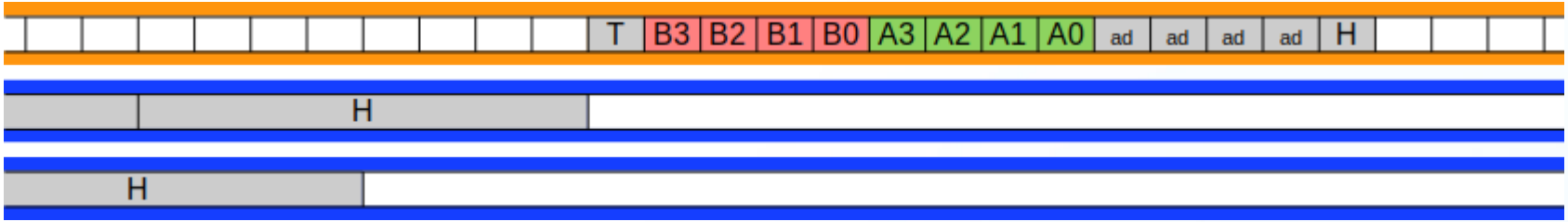


Cost analysis

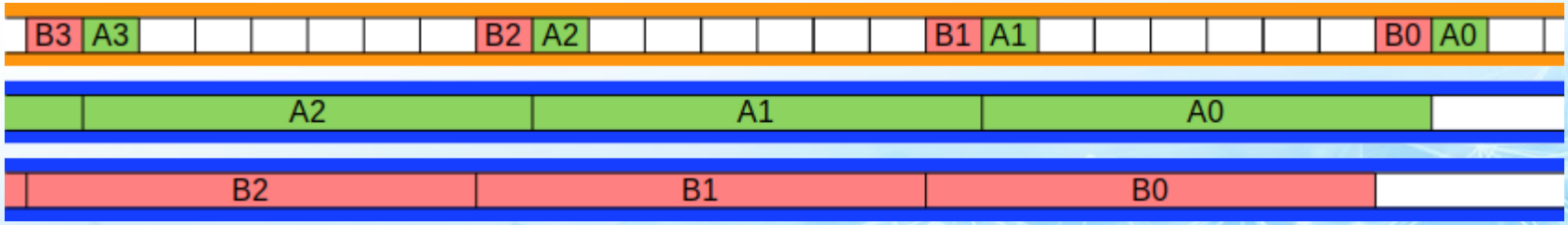
- Intermediate summary
  - Arch. 1: 97x 4 Gb/s MMF → 9,894 €
  - Arch. 2: 112x 250 Mb/s POF → 1,792 €
  - Arch. 3: 9x 4 Gb/s MMF, 112x 250 Mb/s POF → 2,710 €
- BUT additional switch cost in Arch. 3 !
  - Components (HW)
  - Development (SW)
  - Latency
- Protocol has important impact on switch costs in Arch. 3

Cost analysis: protocol impact

- Industry standard protocol: packet based
  - Store packet from 4 Gb/s MMF link. Forward to two 250 Mb/s POF links.



- XC protocol: stream based
  - Straight bit copy (distance 16 (8)) from A and B on MMF link to POF links.



Cost analysis: conclusion

- XC protocol enables simple switches
  - Today: implemented on relatively expensive FPGAs
  - Future: can be implemented on ASIC
    - Marvell Prestera DX multi-port 10 Gb/s silicon is < 100 €
  - Switch cost estimate: 250 €
- Cost summary
  - Arch. 1: 97x 4 Gb/s MMF → 9,894 €
  - Arch. 2: 112x 250 Mb/s POF → 1,792 €
  - Arch. 3: 9x 4 Gb/s MMF, 112x 250 Mb/s POF → 2,710 € + 8x 250 € = 4,710 €
- Cost conclusion for Arch. 3
  - Cost reduction of 50% with same performance
  - PMSiC BOM cost reduction of 7%
  - Simplified supporting software stack

Reliability: bit error rate

- At 1.20 Gb/s on one 4 Gb/s MMF link, on average bit error after 231 hours (9.6 days)
  - with BER = 10^{-15}, usually much better
  - IEEE 802.3 minimum BER = 10^{-12} for links > 2.5 Gb/s (for low MTTFPA)
- With 97 links, on average bit error after 2.38 hours !
- No simple solution
  - Link BER is given and unavoidable technology parameter
  - Not enough time or bandwidth to re-transmit data

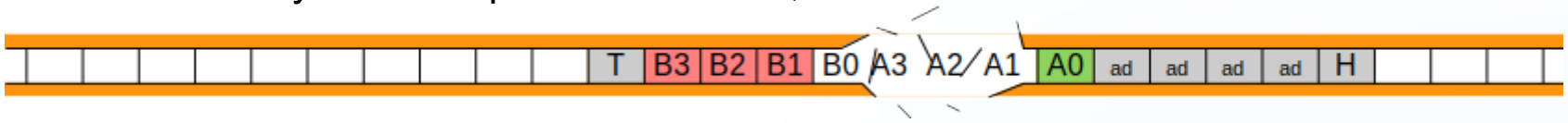
Note: BERs typically given for office environments, not power converters (EN61000-6-3 or FCC 15 class B)

Reliability: bit error correction

- Linear error-correcting codes
  - (3,1), (7,4), (15,11), (31,26) Hamming code is Single Error Correcting (SEC)
  - Add another bit for Double Error Detection (DED)
  - Easily implemented in hardware
  - Example: 11 bits for scheduling of PWM event, 4 additional bits for SEC and 1 bit for DED in 16-bit frame
- Not efficient in practice
  - Errors often occur in bursts (e.g. contactor arcing)
  - Optical cables are immune to EMI, but optical transceivers are not
  - IEEE 802.3 100BASE-TX and 1000BASE-T scramblers → error multiplication

Reliability: protocol impact and conclusion

- Burst error
  - Industry standard protocol: A is lost, B can be recovered with SECDED



  - XC protocol: A and B can be recovered with SECDED

- Reliability conclusion
  - MTBF (theoretically) increased from 2.38 hours to many centuries

Note: This is a theoretical result, since errors should be uncorrelated
→ not always a valid assumption.

Safety

- Equipment safety
  - SFP cage is conductive, requiring grounding for fault currents. 250 Mb/s POF transceiver housing is made from plastic
  - Cost-efficient POF allows safety insulation
- Functional safety
  - Additional channel S can broadcast safety status across all modules in a system
  - Fully implemented as hardware stream. No interference with other streams.
  - Example using a channel S with half data rate of A and B

- Safety conclusion
  - Stream-based XC protocol can simplify system design by enabling functional safety without software support

Conclusion

- XC network development
  - Several years of work, patent pending
  - Aligns with company vision on future of power electronics
  - Current business shows it was a good investment
    - More elaborate systems
    - Higher power levels (and risk !)
    - Meet requirements for cost, reliability and safety
- XC network encompasses components from L3 down to L1
  - L1 (250 Mb/s POF and 16 Mb/s Cu)
  - Avoid licensing issues with existing field bus technology
- Example
  - Cost reduction of 50% on network infrastructure and 7% on PMSiC module
  - MTBF increased from useless 2.38 hours to many years
  - Hardware support for functional safety

Contact

Triphase NV
De Vunt 5
B-3220 Holsbeek
BELGIUM

T: +32 2 669.06.00
E: sales@triphase.com

www.triphase.com