



IEEE COMPEL 2013
The 14th IEEE Workshop on Control and
Modeling for Power Electronics (COMPEL)



From Imagination to Real-Time

Real-Time Simulation of Renewable Energy Systems Using RT-LAB

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Introduction

● When we think about environment and energy, we think:

- Electric Vehicle
- Hydro Power
- Wind Power
- Photovoltaic Power
- Renewable Energies



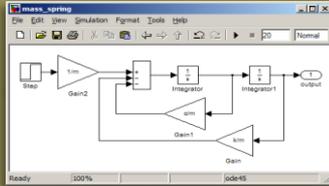
● Power Engineers think about:

- How to control
- How to bring this technology quickly to market
- How to distribute power
- How to interconnect

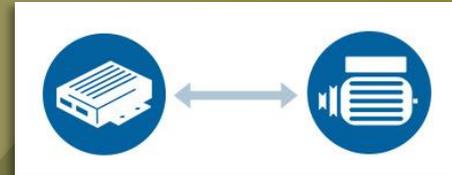
- **Context**
- **Modelling Challenges for Renewable Energy Systems**
- **Solution**
- **Specialized models**
- **Summary**

Context : Real-Time Simulation Helps in Development Process

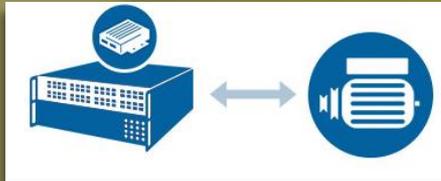
Desktop Simulation



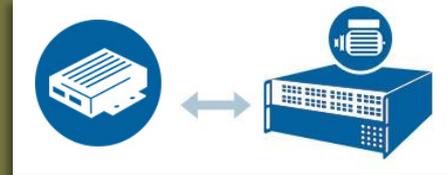
Validation



Rapid Control Prototyping



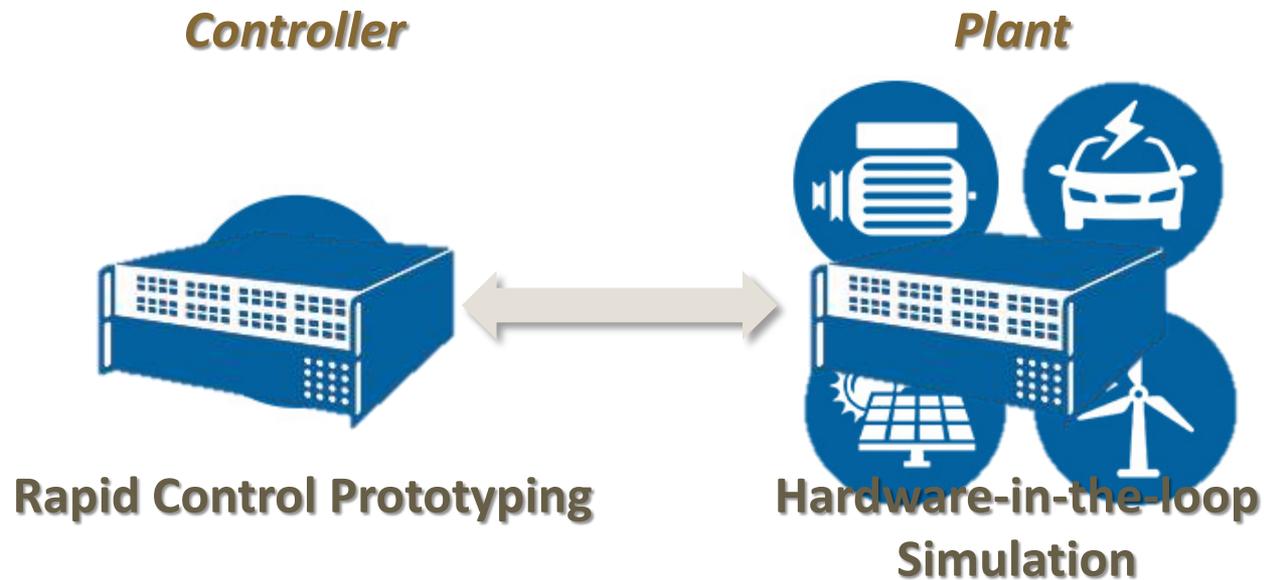
Hardware in-the-loop Testing



Coding



Context : Controlled System, and Real-Time Simulation



Renewable Energy Systems

● **Electric Drive for Hybrid Electric Vehicle and Electric Vehicle**



● **Modular Multilevel Converter (MMC) for HVDC Connection**

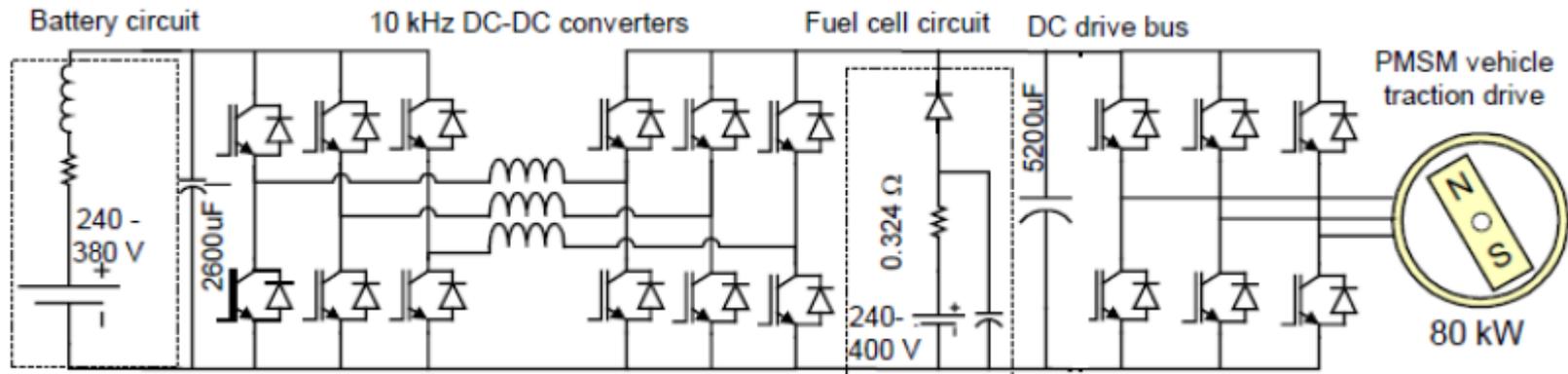


● **Wind farms, Photovoltaic Systems to Grid Connection**



Challenges for Electric Drive

● Example figure : PMSM motor for electric vehicle model



● Reduce latency

- Protection – Fast response needed
- High speed – Fast rotating machine
- Precision – Position of the rotor

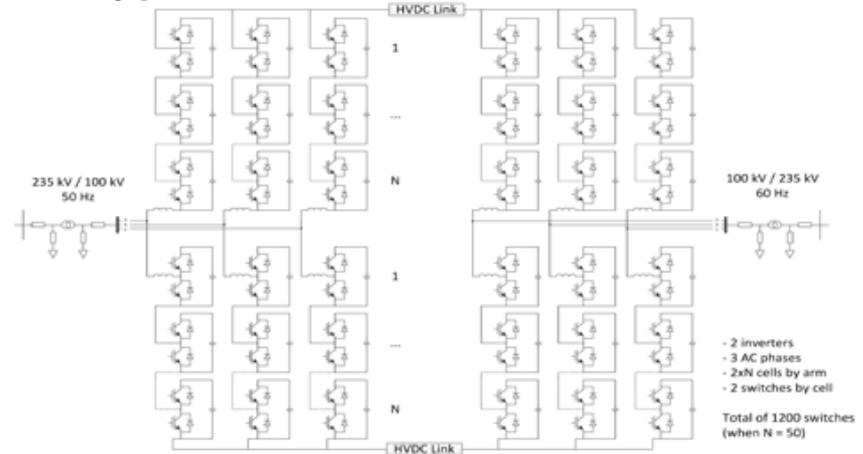
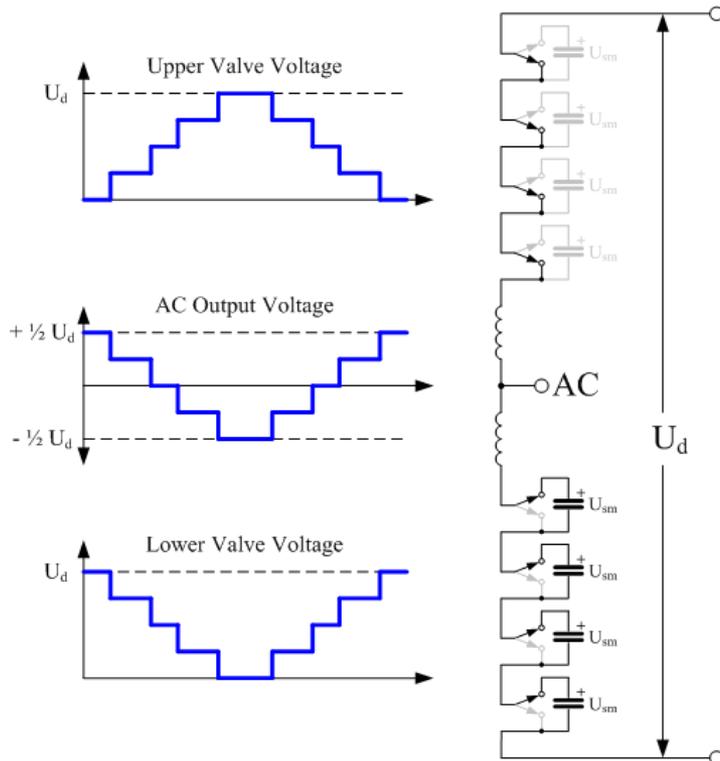


Challenges for Modular Multilevel Converter

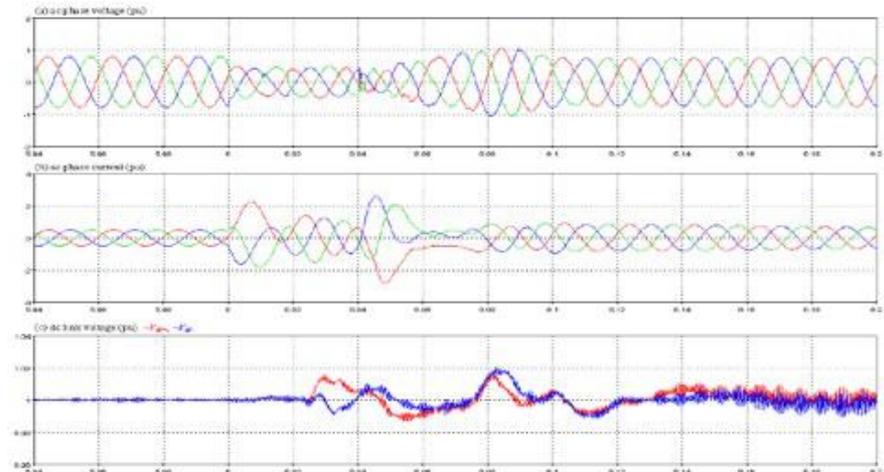


Large number of Inputs/Outputs managements

Typical MMC HVDC circuit



MMC response to a short circuit fault at transformer primary side



CC BY-SA
Wikipedia

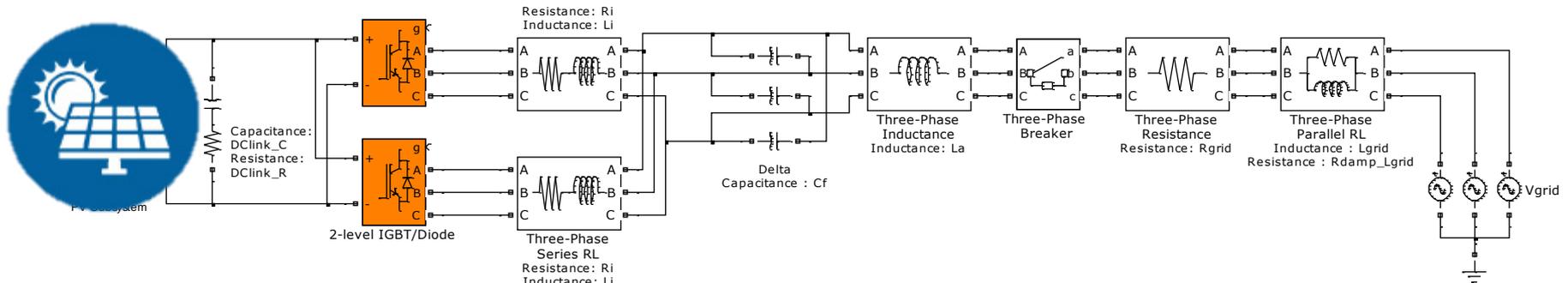
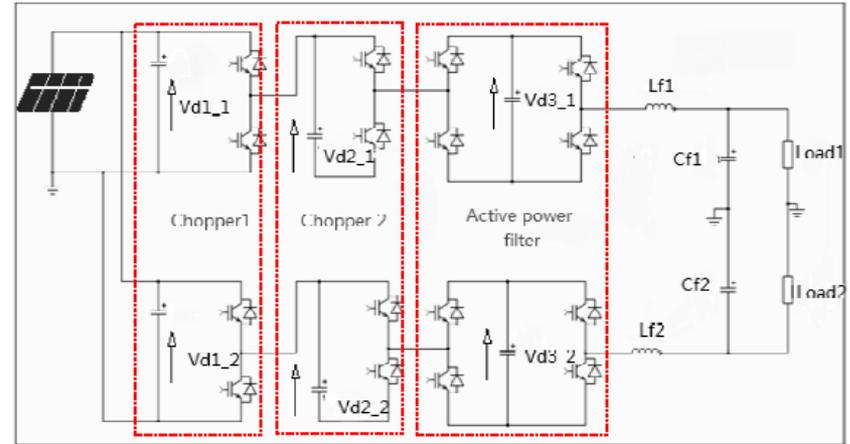
Challenges for Micro-Grid



● Numerous converters

● Fast switching

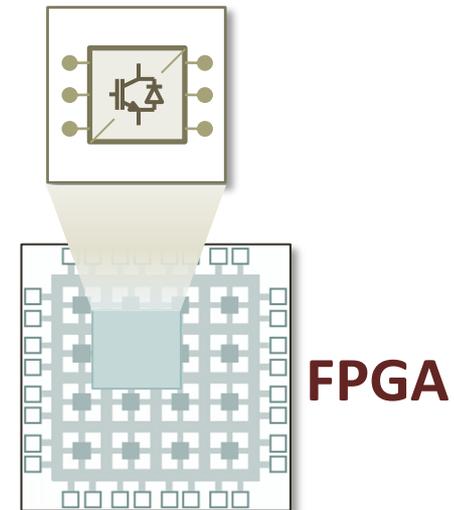
● Short Transmission Lines



Solution : FPGA-based simulation



- **Low Latency**
- **High resolution – Small Time Steps**
- **Non-averaged model**
- **Fault capabilities**
- **Transient analysis**
- **Higher Harmonics effect**





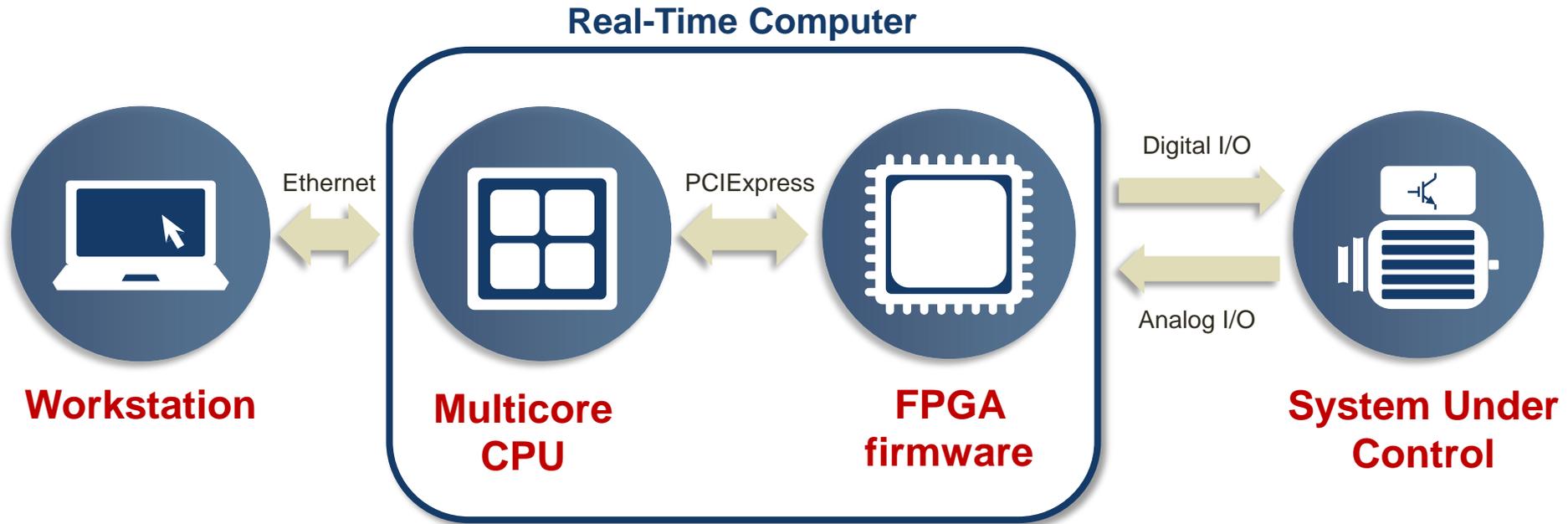
Difficulties

- **FPGA are more difficult to program**
Modeling via Block Diagram
- **Generating bitstream is long**
(typical: 120 min +)
- **Flashing FPGA firmware is long**
~15 mins

Want

- **Easier to program**
- **Flexibility**
- **Save bitstream generation time**
- **Save reprogramming time**

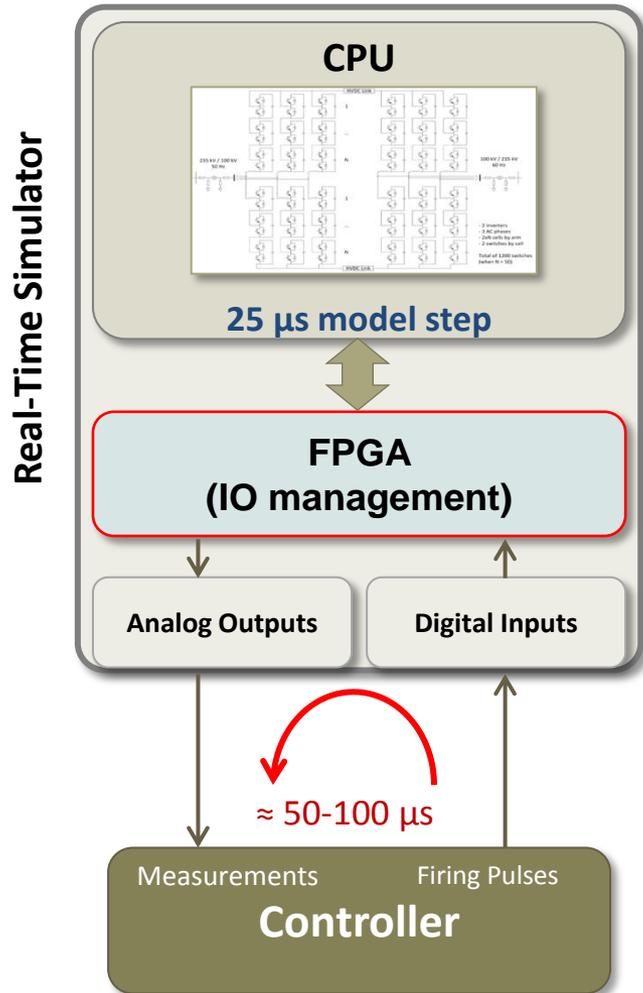
Fast and versatile architecture



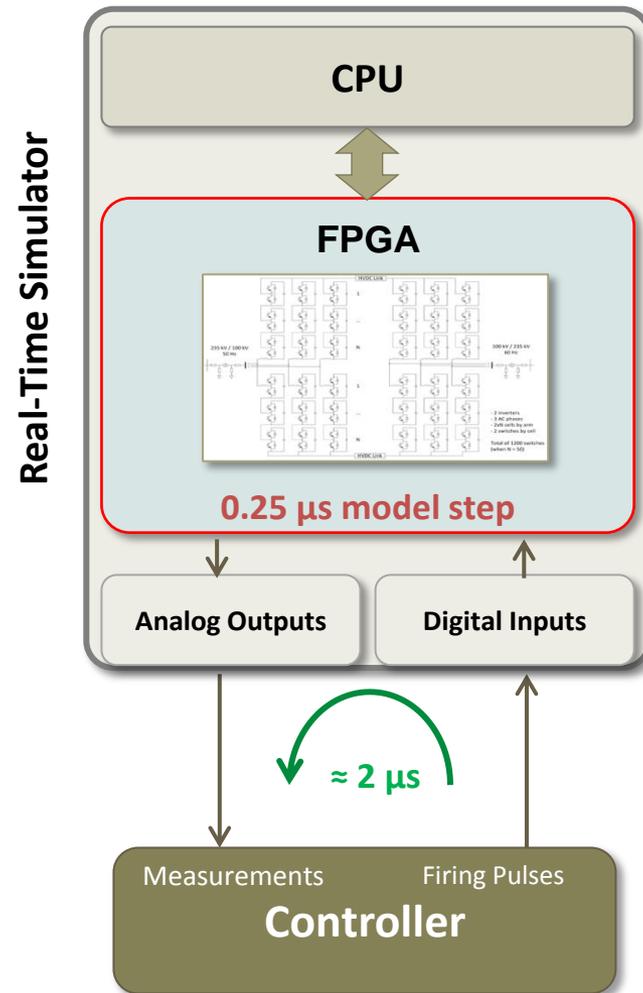
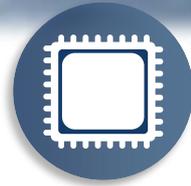
CPU and FPGA-based Simulation Platform



CPU-Based Simulation



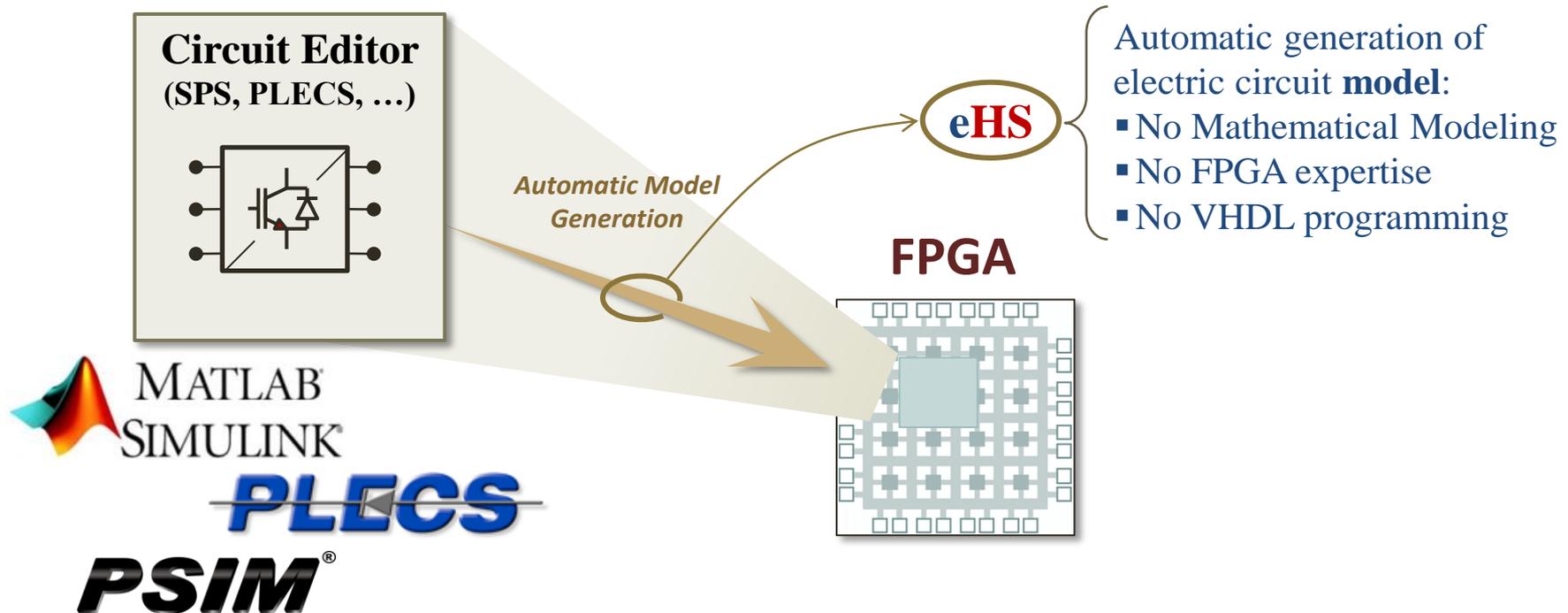
FPGA-Based Simulation



eHS Key Features

● eHS (electrical Hardware Simulation) solver

- Generic Power Converter solver on FPGA
- SPS model editor interface (Soon with PLECS, PSIM and EMTP-RV)
- Reconfigurable from Host PC without reprogramming the FPGA
- Simulation in off-line mode with eHS nodal solver within Simulink



eHS Nodal Solver

● eHS uses the modified nodal analysis approach

- It solves a admittance matrix to find the voltage at each node and the current from each sources.
- The admittance matrix does not need to be re-computed for each switch status
- Simulated model topology and parameters can be modified without recompiling the bitstream

● The maximum size of the circuit is determined by the number of inputs, switches and reactive components

● Currently, the maximum number of components is :

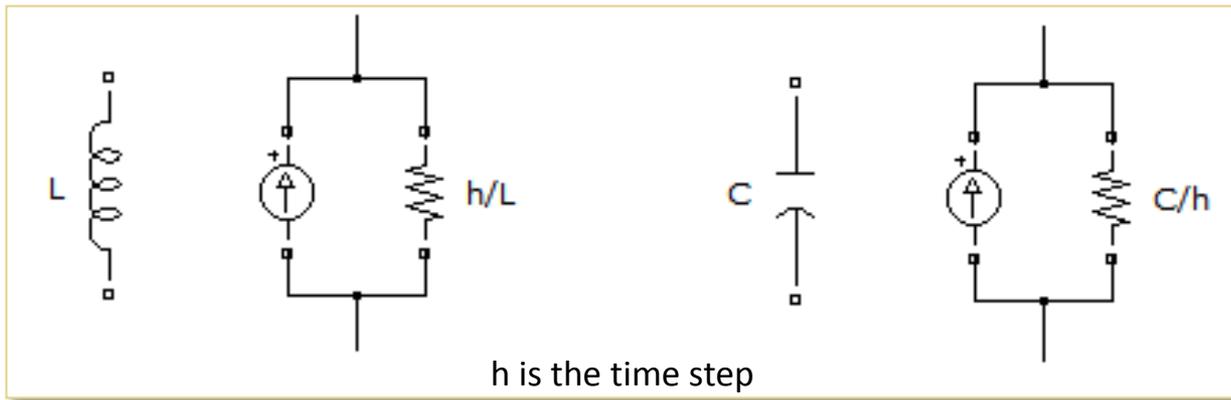
- 16 inputs (voltage/current sources)
- 16 outputs (voltage/current measurements)
- 24 switches (IGBTs, breakers, etc)
- 60 non-switching devices (ie. L and C) – unlimited resistors



Switch Model in eHS

● eHS method replaces switches by:

- either a very small inductance when conducting
- or a very small capacitor when not conducting



- This method is called the fix-Y because the admittance matrix does not change when a switch changes state.

Switch Model in eHS

- For the matrix to remain the same upon switching event, the following equation must remain true

$$G_s = h/L = C/h \quad \text{where } h \text{ is the time step}$$

- When building the nodal matrix a value between 10 and 0.001 has to be set to represent a switch. This determines the value of the inductor and the capacitor representing the switch.

$$L = h/G_s \qquad C = h \times G_s$$

- For example, a time step 100ns and a $G_s=1$, the switch will be represented by the following inductance when conducting or the following capacitance when non-conducting.

$$L = h/G_s = 100\text{ns}/1 = 100\text{nH} \qquad C = h \times G_s = 100\text{ns} \times 1 = 100\text{nF}$$

- Ideally, we need a very small inductor and a very small capacitor to represent an ideal switch. Depending on the circuit topology, the best result is obtained by optimizing the value of G_s and comparing results with conventional off-line software.

Difficulties

- **FPGA are more difficult to program**
Modeling via Block Diagram
- **Generating bitstream is long**
(typical: 120 min +)
- **Flashing FPGA firmware is long**
~15 mins
-

Want

- **Easier to program** 
- **Flexibility,**
freedom to change circuit topology 
- **Save bitstream generation time** 
- **Save reflashing time** 
- **On-line modification of circuit parameters**
- **On-line modification of circuit topology** 

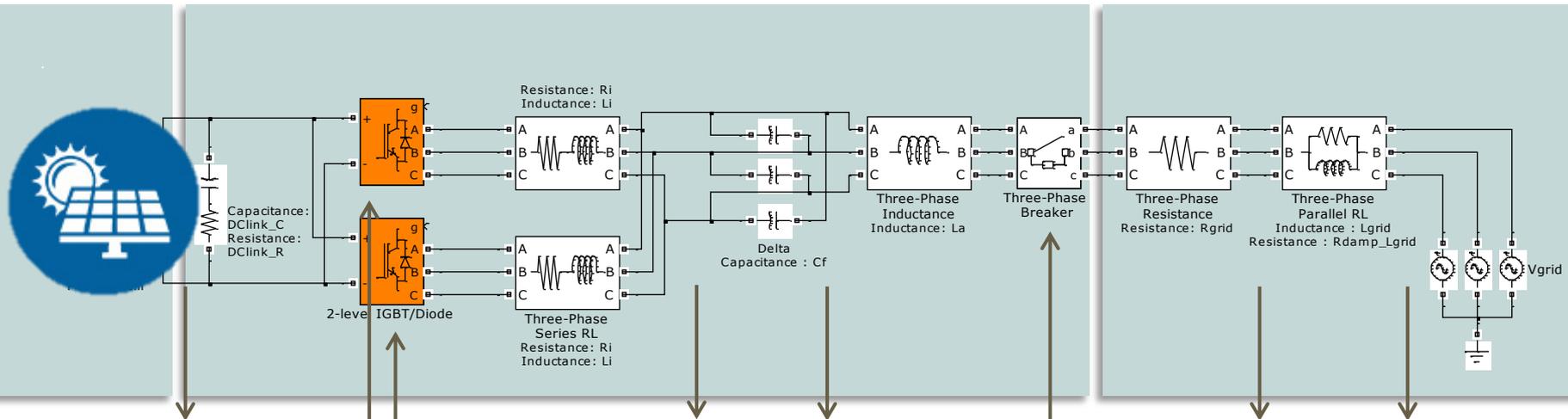
Real-Time eHS Simulation Examples

eHS model : PV connected to grid.

CPU

FPGA (500 ns)

CPU (20 μ s)

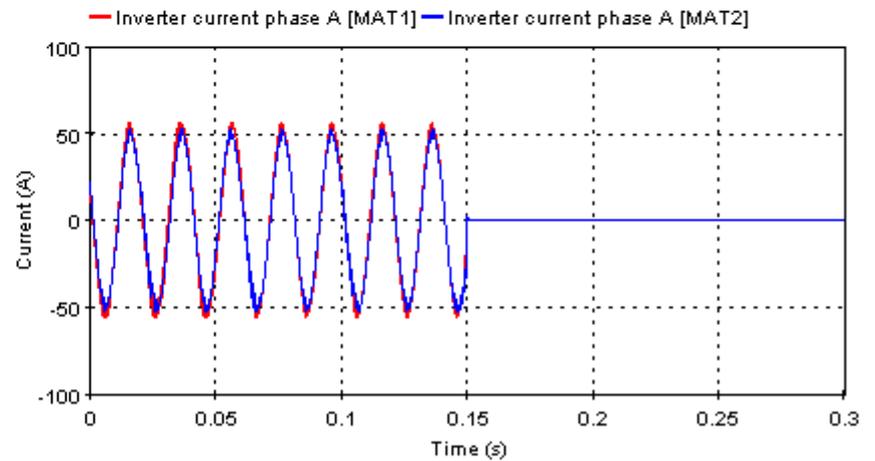
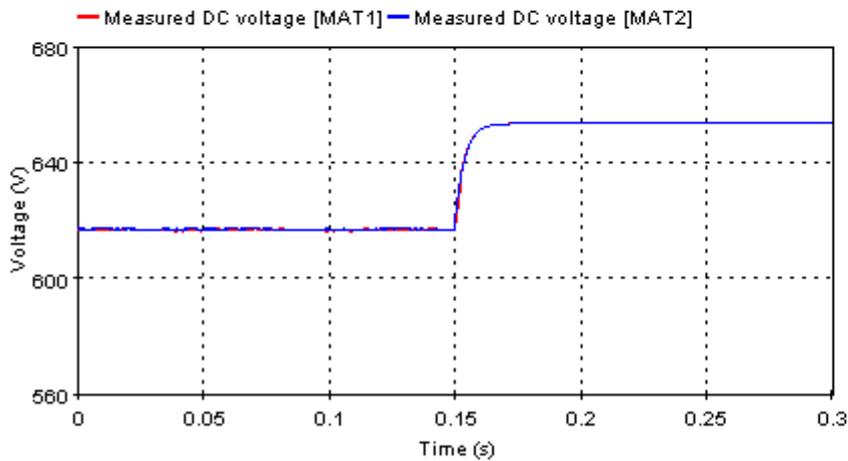
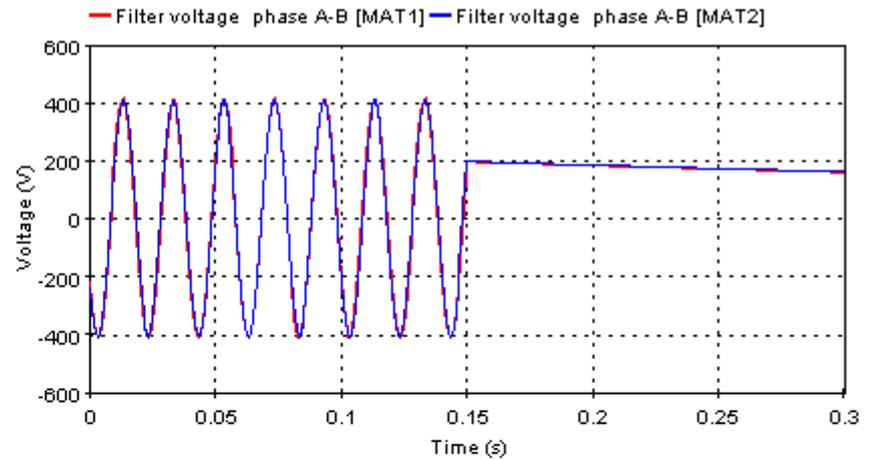
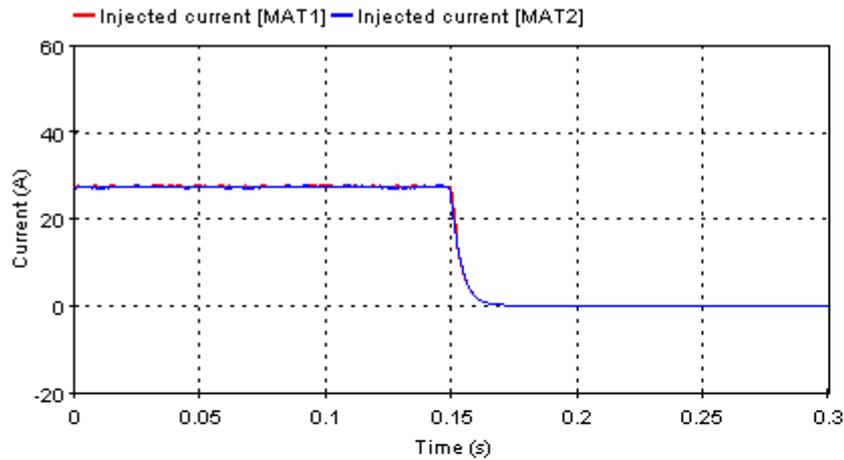


CONTROLLERS (On CPU, FPGA or using external hardware)

- Time Step = 500ns
- 4 sources inputs (1 DC from PV, 3 phases AC from Grid)
- 16 voltage and current measurements,
- 15 switches (2x 2level inverters & 3phase breaker)

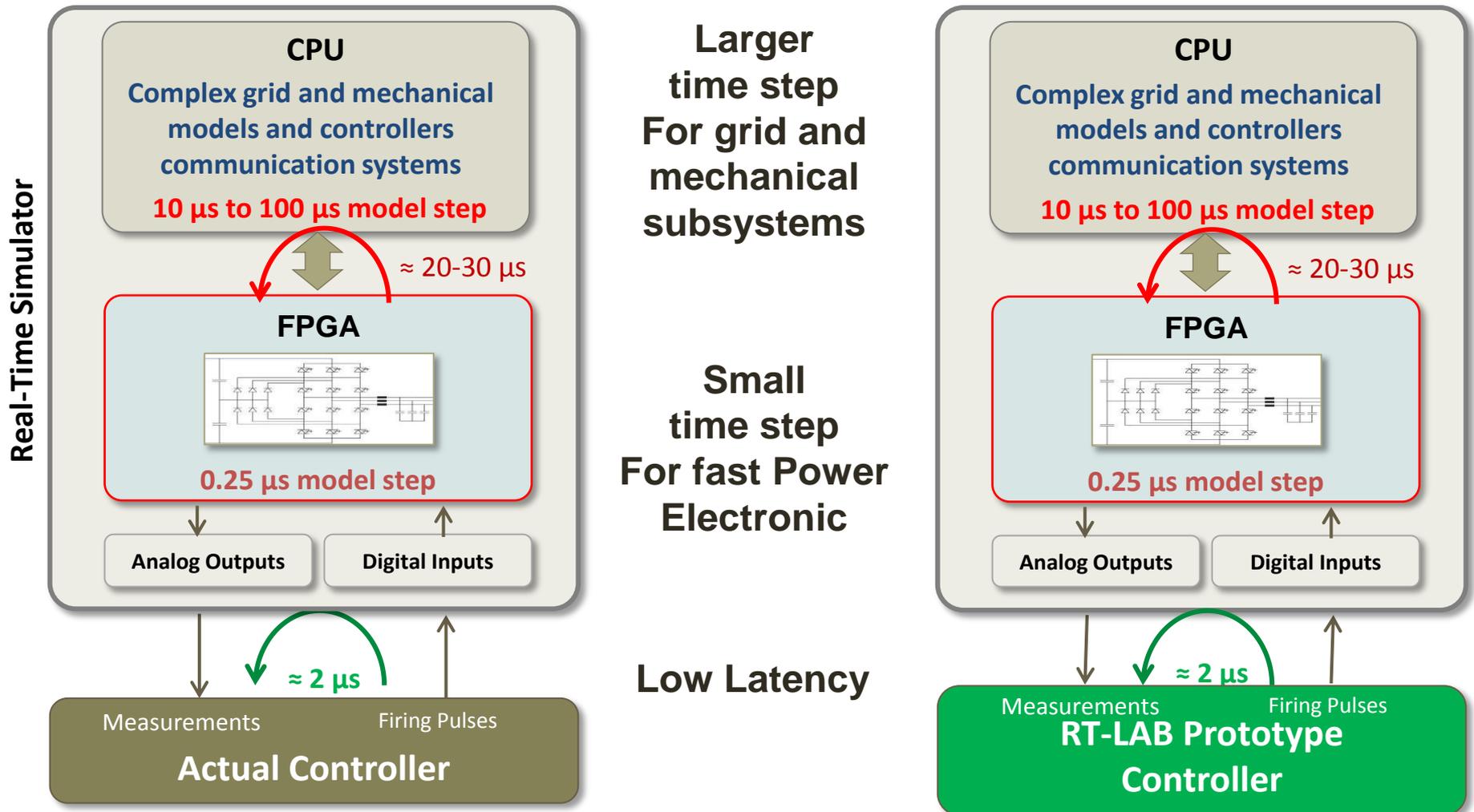
Real-Time eHS Simulation

Results for PV model



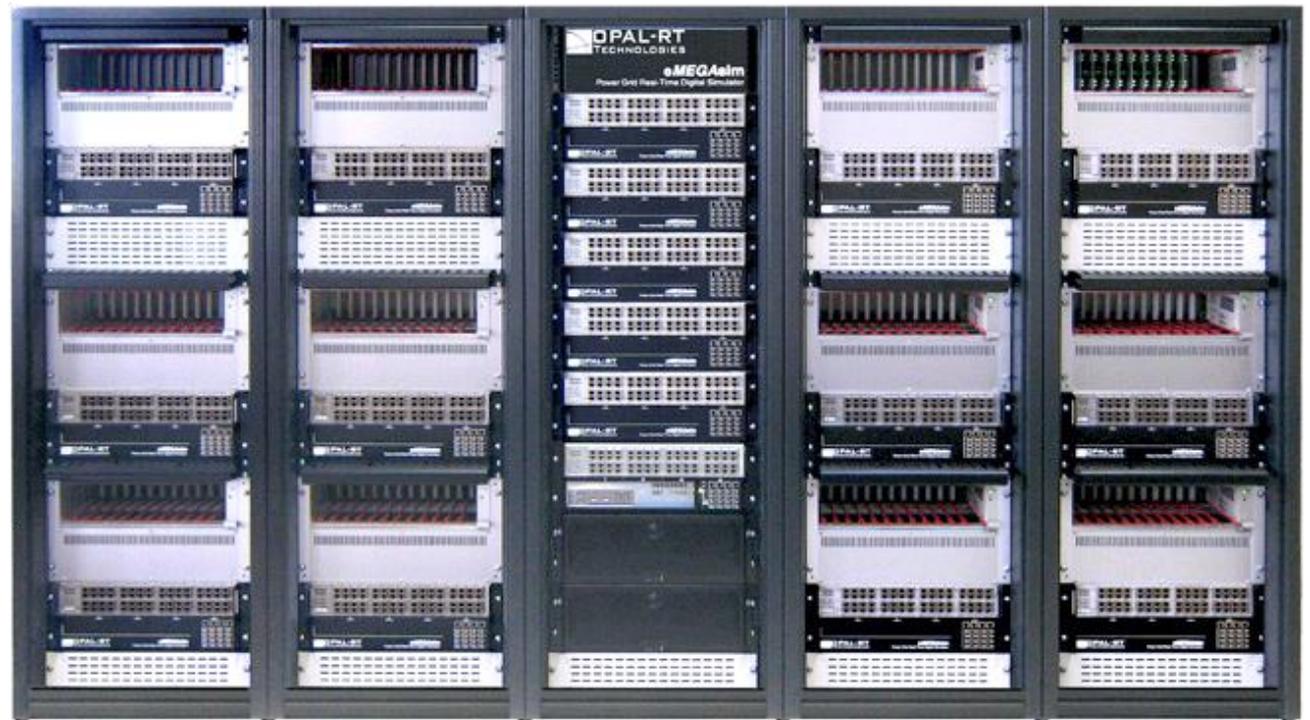
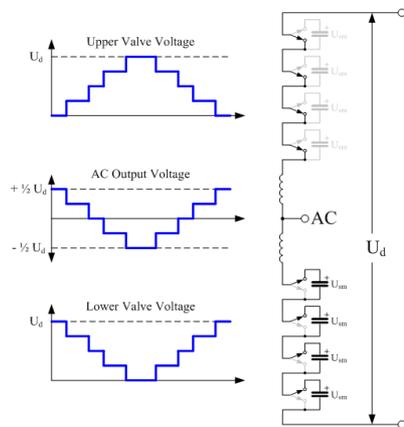
Mixed CPU-FPGA-based Multi-Rate Simulation Platform

Standard architecture of OPAL-RT RT-LAB simulator and RCP system



Specialized Models

MMC Solver



Specialized Models

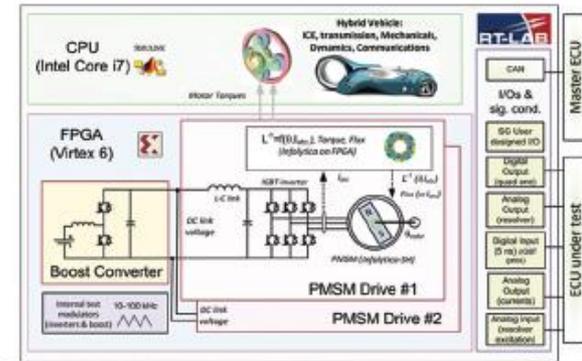
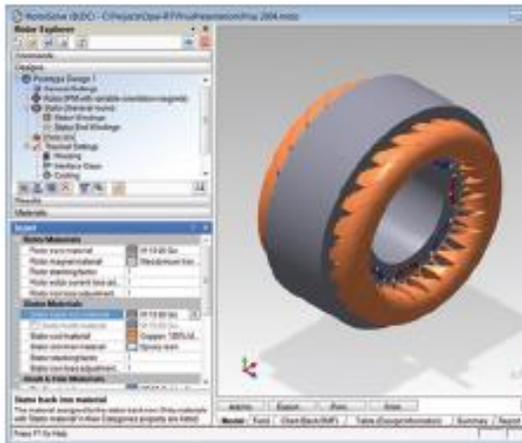


Motor model on FPGA

- Using Finite Element Analysis (FEA) modeling approach:
 - Such as JMAG-RT and MotorSolve

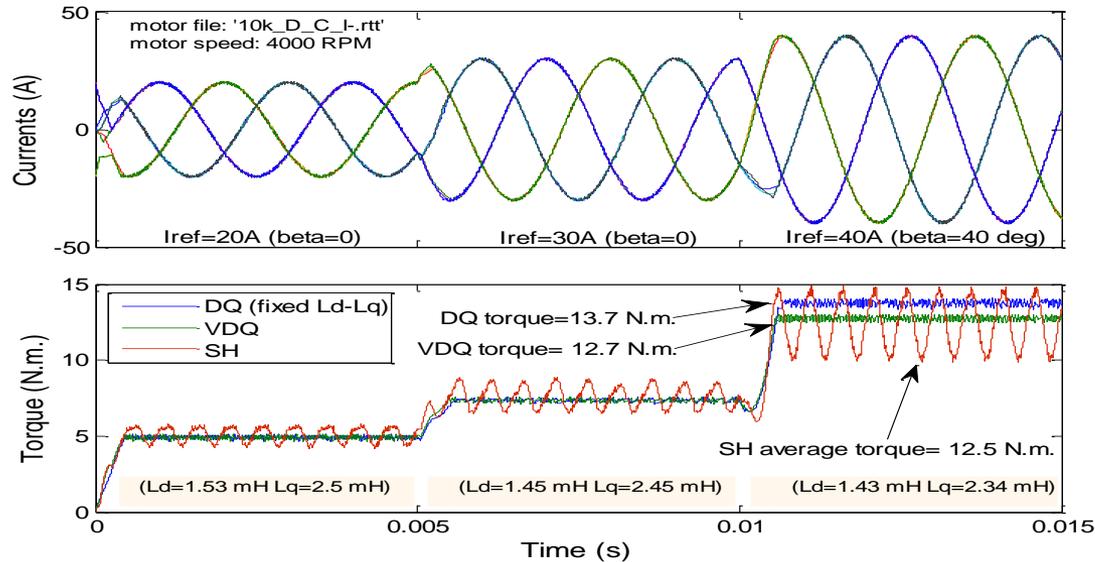
Flux, impedance values according to the mechanical angles of the motors

Motor Parameter File



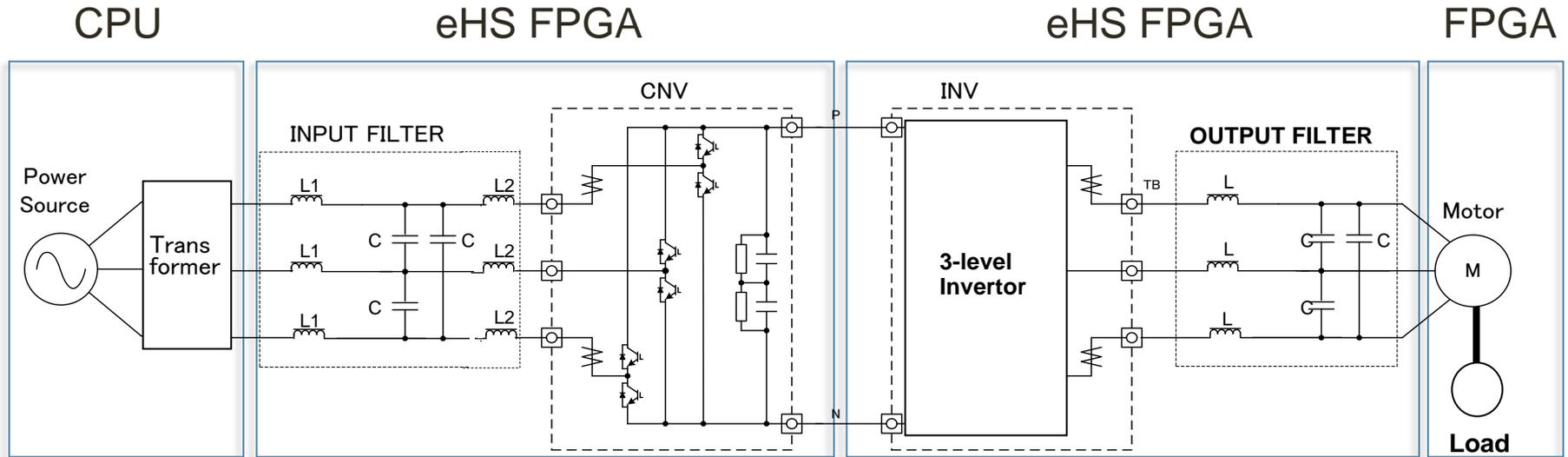
Specialized models

Comparative results :



✓ Torque control results at high currents (saturation)

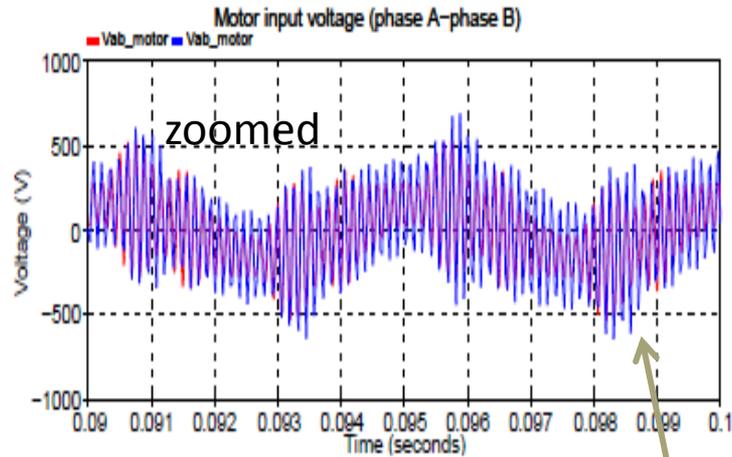
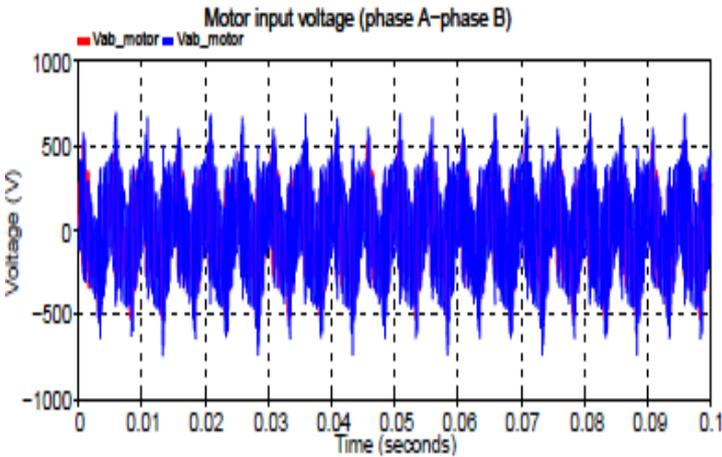
Real-Time FPGA-based Simulation Example



eHS Real-Time (eFPGAsim, Virtex 6)

- Ac side & Converter: 400 ns
- Inverter & Filter: 690 ns
- FPGA PMSM motor: 100ns
- Inverter switching frequency = 8 kHz
- Converter switching frequency = 4 kHz

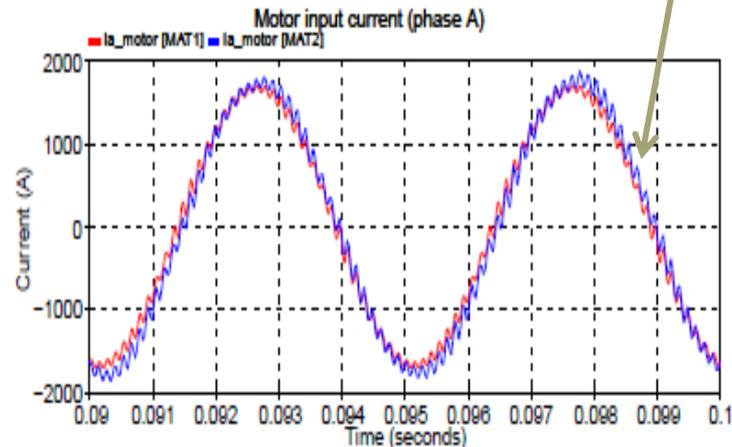
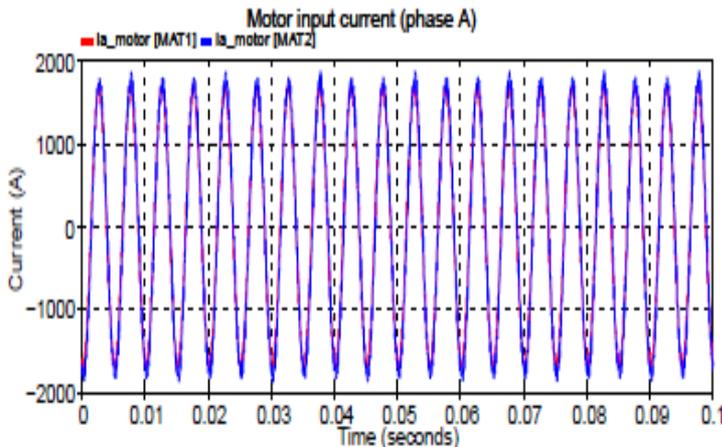
Real-Time FPGA-based Simulation Example



**Motor voltage
(Phase-to-phase)**

eHS and SPS
superimposed

8-kHz components due to the 8-kHz PWM carrier



Motor current

eHS and SPS
superimposed

OPAL-RT FPGA-based Simulation

Non-Flashing technology:

- 1 firmware by application which handle a large number of configuration

Motor Type : JMAG 10.5 PMSM Spatial Harmonics rtt file

Rtt file Path :
`'10k_S_C_I.rtt'`

Park transform for Id Iq scaling : quadrature transform (with s

Multiple configurations:

- Generic Power Systems solver
- Modification in a model editor
- Reconfigurable from the host PC

Function Block Parameters: PMSM Motor SH

eFPGAsim PMSM motor Spatial Harmonics Block (mask) (link)

This block processes the communication between the RT-Lab model and the FPGA motor model. It also initialises the FPGA motor solver with the user motor definition file.

It supports multiple file type :
-JMAG v10.5 rtt files
-Infolytica motor mat files

General Motor1 Motor2

Motor Type : JMAG 10.5 PMSM Spatial Harmonics rtt file

Rtt file Path :
`'10k_S_C_I.rtt'`

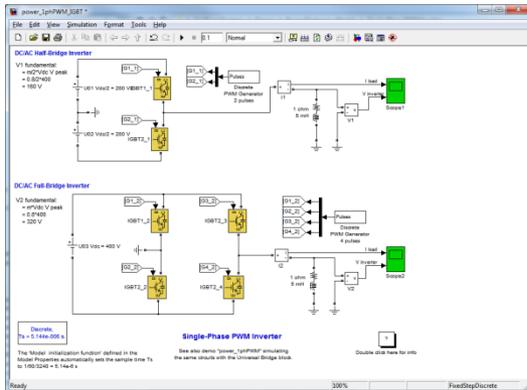
Park transform for Id Iq scaling : quadrature transform (with $\sqrt{2/3}$ factor)

Rotor flux position when Theta = 0 : 90 degrees behind phase A axis (modified Park)

Use advance table settings

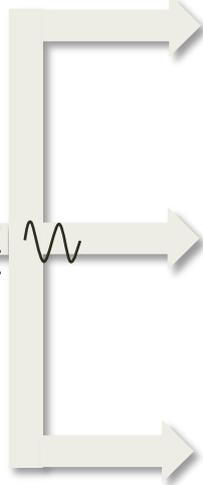
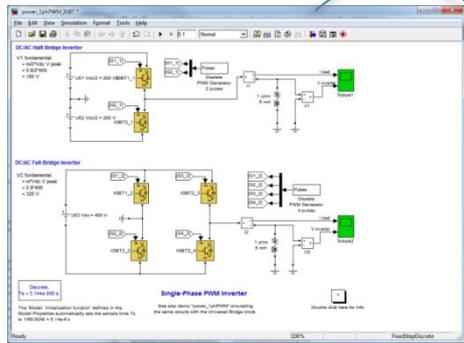
Vabc filter cut-off Frequency : [Hz]
10000

OK Cancel Help Apply



OPAL-RT Real-Time Simulation

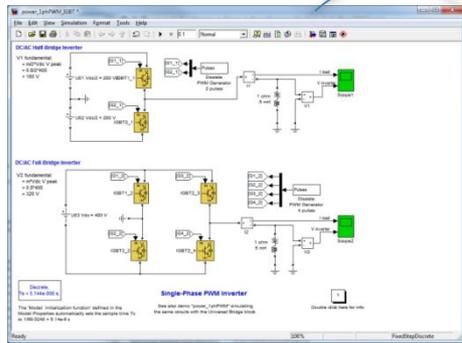
Flexible I/O routing and configuration



The screenshot shows several configuration panels in the OPAL-RT software. The top panel is a table for 'C1d Signal' with columns for 'In', 'Gain', 'Other', 'Min', and 'Max'. Below it are panels for 'HORIZ SPEED MODE', 'SOURCE MODE', and 'PVAL PARAMETERS'. The 'HORIZ SPEED MODE' panel has a dropdown menu set to 'Use the Mechanical Feedback'. The 'SOURCE MODE' panel has a dropdown menu set to 'Use Gate Signal from DIN'. The 'PVAL PARAMETERS' panel has several input fields for 'Modulation Index (0-1)', 'F gain (Hz)', 'Angle (Deg)', and 'Area (Cm2)'. The bottom right corner shows a small logo.

OPAL-RT Real-Time Simulation

Flexible I/O routing and configuration



The screenshot shows the configuration interface for the OPAL-RT hardware. It includes sections for "Signal", "Hardware", "Source", and "PDU Parameters".

Signal	Hardware	Source	PDU Parameters
Ch1 Signal: In, Out, Other, Max, Min, On	Ch1 Signal: In, Out, Other, Max, Min, On	Ch1 Signal: In, Out, Other, Max, Min, On	Simulation Error (Stop), F gain (Hz), Ch1 Time (ms), 100.0, 0.0
Ch2 Signal: In, Out, Other, Max, Min, On	Ch2 Signal: In, Out, Other, Max, Min, On	Ch2 Signal: In, Out, Other, Max, Min, On	
Ch3 Signal: In, Out, Other, Max, Min, On	Ch3 Signal: In, Out, Other, Max, Min, On	Ch3 Signal: In, Out, Other, Max, Min, On	
Ch4 Signal: In, Out, Other, Max, Min, On	Ch4 Signal: In, Out, Other, Max, Min, On	Ch4 Signal: In, Out, Other, Max, Min, On	

Additional settings include: HORIZ SPEED MODE (Use the Mechanical Feedback), SOURCE MODE (Use Gate Signal from SW), VDC MODE (From a constant value), and CH1 VDC value (0 Vdc).

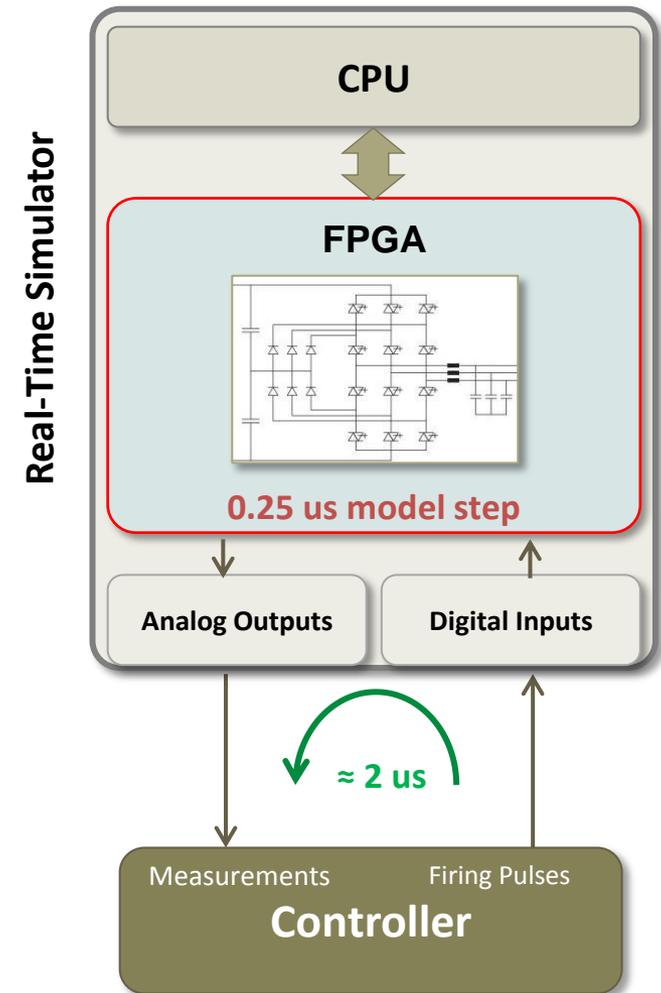
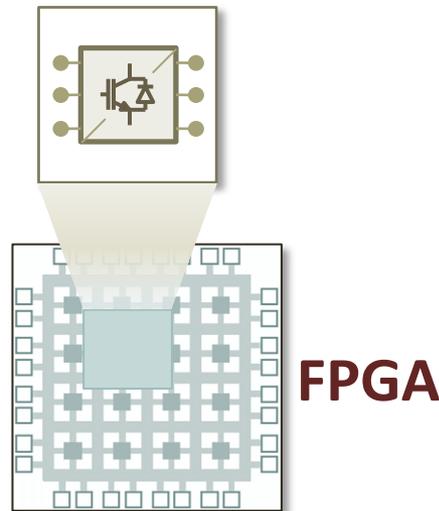
Summary

FPGA-based Simulation has many advantages over regular CPU-based simulation

- High Resolution Simulation
- Low Latency

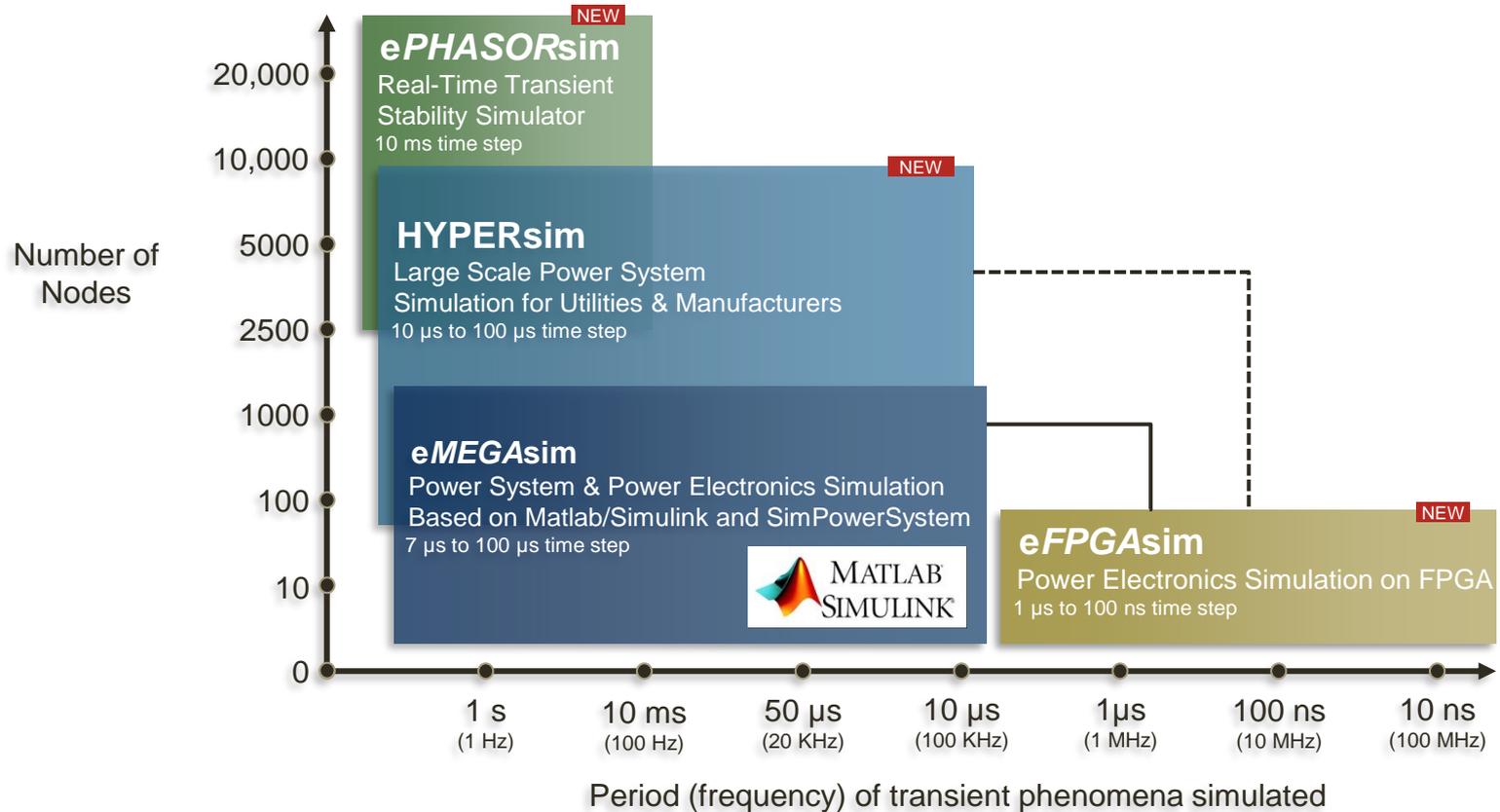
With OPAL-RT's eFPGAAsim, modelling is :

- Easy
- Reliable
- Flexible
- Customizable



ePOWERgrid Product Family

● Cover the complete spectrum of power system analysis & studies





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From Imagination to Real-Time

Real-Time Simulation
of Renewable Energy Systems
Using RT-LAB

Thank you !

Presented by Andy Yen

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