

EHS QUICKSTART GUIDE EFPGASIM TOOLBOX RTLAB / CPU SECTION

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INTRODUCTION

The eHS solver is an FPGA-based technology developed by OPAL-RT for real-time power electronics simulation. Thanks to a convenient circuit schematic graphical user interface, the FPGA code is automatically generated, making FPGA-based simulation accessible to a large number of users.

This document provides basic information on how to create a new project with a template that includes the eHS solver and how to run a real-time simulation with an example model included in the template. The guide is designed for the OP45xx and OP56xx targets.

REQUIREMENTS

OPAL-RT HARDWARE

- OP4500 / OP4510 / OP4520
- OP5607 / OP5600 / OP5707

RECOMMENDED OPERATING SYSTEM

Microsoft Windows 7 64bits Version 6.1 (Build 7601: Service Pack 1)

PRE-INSTALLED SOFTWARE

The following software must be installed and functioning to perform the tests described in this document. Confirm that the required software is installed and test to ensure they are functioning properly.

Type >> ver on the MATLAB prompt and verify that you have the following toolboxes (or later versions of them) installed.

Recommended configurations for basic use (only circuit simulation):

- •MATLAB 2011b / 2013a / 2015aSP1, 32-bit version
- •RT-LAB v11.1.3 or later
- •At least one of the following tools:

SimPowerSystems "Specialized Technology" Simulink library
 Powersim PSIM v9.3.4 or v10.0.6 (v10.0.5 is unsupported)
 Plexim PLECS Simulink Library v3.7.4
 NI Multisim 13

The RT-XSG toolbox requires the following software to generate programming files for reconfigurable devices and to program the platform:

Recommended configuration for firmware generation, for Xilinx 7 series:

- •MATLAB 2015b, 64-bit version
- •Xilinx Vivado suite 2015.3 & Xilinx Vivado System Generator for DSP 2015.3
- •RT-XSG v3.1.2 or later

LICENSED RT-LAB COMPONENTS

You must have licenses for the following RT-LAB components to run the examples provided in this document. Verify with your sales representative that your system includes these licenses.

RTLAB_RT	RTLAB_XHP	RTLAB_DEV	RTLAB_NUM_CORES >= 1
RTE_RT	RTE_NUM_CORES >= 1	XSG_EHS	



RUNNING A MODEL ON OP45XX/OP56XX TARGETS

CREATING A NEW RT-LAB PROJECT

Open RT-LAB and follow these steps to create a new RT-LAB project:

- 1. In the main RT-LAB User Interface, navigate to File > New > RT-LAB Project to open a new project wizard.
- 2. Enter a project name (e.g. eHS_examples), then click Next.
- 3. Browse the template directory to select the model to add it to the project. Open the *eFPGAsim* folder and select **eHS with IOs > OP4510 > eHSx64_with_IOs_on_OP4510 (Simulink).**
- 4. Click Finish to create the new RT-LAB project in the project explorer.

9 F	RT-LAB				
File	Edit Navigate Search Sim	ulation	Run To	ools	Window Help
1	New			• 😕	RT-LAB Project Quick Access 🗈 Edition
1	Open File Quick Start-up project			₹ 	RT-LAB Model
	Close All	Ctrl+S	Ctrl+W hift+W		
	Save Save As		Ctrl+S		(2)
1	Save All Revert	Ctrl+	Shift+S		New RT-LAB Project
	Move		50		Create a new RT-LAB project. This project can be generated from a template.
8	Refresh		F2 F5		Project name: eHS_examples
4	Print Switch Workspace		Ctrl+P		Use default location Location: C\Users\deniselefebvre\OPAL-RT\RT-LABv11_Workspace\eHS_exam Browse Browse
èь cá	Restart Import Export			. S	Project description:
	Properties	Al	t+Enter		Add project to working sets
£	Open Log Viewer				Working sets: Select
۷	Exit and reconfigure for 10.X Exit				0
			•		Cancel

Figure 1: Creating a new project

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 OP4500 OP4500 		
eHSx64_with_30s_on_OP4510	1	and the providence of the second second
▶ (2+) OP5607		
> 2 eHSi64_Gen3		Description
a) eHSu15 DiodeBridge		Description
eHSut6_Two_Level_Inverter		This model illustrates the use of the eHS solver to compute the outputs of a three-phase
eHSu64_Diode_Bridge	-	load. It is intended to demonstrate the interconnection of the eHS solver with advanced I/O
Features		with an external device.
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		<u> </u>

Figure 2: Browsing model templates



The *eHS_examples* project will be created and the corresponding RT-LAB model will be imported into the project workspace (in this example, the model is named *Converter3Phase3LevelNPC_OP4510_rtlab*).

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No operations to display at this time.	No selection	
		P.

Figure 3: Example workspace



EDITING THE MODEL

Before building the model, verify that you can access and edit the model.

Click on **Edit the model** in the *Preparing and Compiling* pane. The model file will be opened in a new MATLAB/Simulink window.

Name: Converter3Phase3LeveINPC_OP4510_rtlab Path: C:/Work/My_RTLAB_Workspace/eHS_exam Matlab: R2010B State: Not loadable <not compiled=""> escription: Executing Executing Set the execution pr Set the execution pr Three NPC Converter example model Executing Three NPC Converter example model Set the execution pr Three NPC Converter example model Executing Three NPC Converter example model State: Set the execution pr Three NPC Converter example model</not>	eneral Info	rmation	Preparing and Compiling	
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	escription:		Executing Set the execution pr Set the ex	Interfer example model

Figure 4: Editing the model

MODEL DESCRIPTION

The model is composed of two main subsystems:

- 1. SC_Console: Subsystem executed by the host computer during the simulation to monitor and control the simulation.
- 2. SM_Controller_eHS_IOs: Subsystem executed by the target simulator, in real-time, on the system CPU that communicates with the FPGA board and the physical system I/Os.







SC_CONSOLE

Double click on the **SC_Console** to open the SC_Console details window.



Figure 6: Model SC_Console window



SM_CONTROLLER_EHS_IOS

Click on the **SM_Controller_eHS_IOs** to open the SM details window. This window provides a detailed diagram of the master subsystem.



Figure 7: Model SM_Controller_eHS_IOs window



EHS GEN3 COMMBLK

The *eHS Gen3 CommBlk* communicates with the FPGA board to initialize the eHS core. During real-time operation, it provides eHS inputs (the circuit Sources / Gates control signals) and reads the eHS outputs (current and voltage measurements) at the RT-LAB model rate.



Figure 8: eHSx64 Gen3 CommBlk diagram

The user must provide a circuit file (SimPowerSystems Simulink model, PSIM file, PLECS Simulink model, or NI Multisim 13 XML netlist) to declare the circuit that will be simulated inside the eHS core.

In this example, the circuit file is a SimPowerSystems Simulink model named *Converter3Phase3LevelNPC.mdl*.

Function	Block Par	ameters: eHSx64 Gen	CommBlk			х
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This block power-ele sample ra The netlis (.psimsch The block switches. In additio	c allows t ectronic c ate that t st file can) or a Mu c enables n, it does	the configuration an circuit. The eHSx64 he RT-LAB system. be either a SimPov ultisim netlist (.xml) real-time control of s the scenario mana	d the control of a Gen3 core is locat werSystem (SPS) o). f its voltage and co agement of the ne	eHSx64 Gen3 solver to con ed on an FPGA-based boar or PLECS simulink model (.r urrent sources as well as th tlist.	npute the outputs of a d and runs at higher ndl), a PSIM netlist ne gate signals of the	
Circuit	Infos	Inputs Settings	Gates Settings	Scenario Management	Comm Settings	
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Circuit file	name					
Converter	3Phase3	LevelNPC				
Provide Sample tir	explicit : me for el-	sample time for solv IS	ver eHS (otherwis	e use optimal value)		
3e-007						
Show a	dvanced	settings for eHS so	lver			
•			111			•
				OK Cancel	Help App	ply

Figure 9: Block parameters window



CIRCUIT FILE

The circuit file models an NPC converter. The eHS solver will extract the components netlist from this file and calculate the system equations before running them on the FPGA board.



Figure 10: Model converter diagram



VALIDATING THE MODEL

Run an offline simulation from the RT-LAB model to ensure that all the library links are resolved using your MATLAB instance.

Verify that the model runs properly.

• In RT-LAB, check that your target is available in the Targets list, and is up and running (any problems with the target will be displayed by RT-LAB as an icon change and added text after the target name).



• Right-click your target and select Set as development node

<RT-LAB not installed>

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4 🐸 eHS exa		Open	eneral Informat	tion	Operations		
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+ Create		Paste Ctrl+V	IP address:	192.168.1.65	Execute a Python script on this target.		
	×	Delete Delete	State:	qU	I Flash an I/O board with a bitstream.		
		Rename F2	License:	Activated	Execute a custom command.		
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		Tools	▶ arget Number.	PF000-000-301	X Clean the core dumps.		
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		Install	•				
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Figure 11: Setting the target as development node



 Click on the License tab to display the list of software licenses and make sure that XSG_EHS, RTLAB_RT, RTLAB_DEV, RTLAB_XHP and RTE_RT licenses are enabled. You must also have at least RTLAB_NUM_CORES and RTE_NUM_CORES >= 1.

-LAB License Features			
Feature name	Version	Status	Description
RTLAB NRT	11.0	enabled	Allows to execute a model in non real-time mode
RTLAB_NUM_CORES	11.0	12 enabled	Allows to execute a model in non real-time mode with RT-LAB.
RTLAB_RT	11.0	enabled	Allows to execute a model in real-time mode with RT-LAB.
RTLAB_XHP	11.0	enabled	Enables the XHP mode within RT-LAB.
RTLAB_ARINC429	11.0	enabled	Enables ARINC429 protocol option.
RTLAB_C37_118_MASTER	11.0	enabled	Enables C37.118 master protocol option.
RTLAB_C37_118_SLAVE	11.0	enabled	Enables slave Synchrophasor Protocol C37.118.
RTLAB_COMM_FW	11.0	enabled	Enables to distribute simulation over a cluster of target using Firewire realtime link.
RTLAB_COMM_SCI	11.0	enabled	Enables to distribute simulation over a cluster of target using Dolphin realtime link.
RTLAB_DEV	11.0	enabled	Allows to compile a model.
RTLAB_DNP3_SLAVE	11.0	enabled	Enables slave Distributed Network Protocol (DNP3).
RTLAB_FIELDBUS	11.0	enabled	RTLAB_FIELDBUS
RTLAB IO 61850	11.0	enabled	Enables IEC61850 communication protocol for protection relay interface.
RTLAB KETEREX 12C	11.0	enabled	Enables Keterex I2C communication protocol.
RTLAB KETEREX SPI	11.0	enabled	Enables Keterex SPI communication protocol.
RTLAB OPC	11.0	enabled	Enables Open Platform Communications (OPC) protocol.
RTLAB ORCHESTRA	11.0	enabled	Enables Orchestra co-simulation framework.
RTLAB SPECTRACOM TSYNC PCIE	11.0	enabled	Enables GPS synchronization with the Spectracom TSvnc PCIe card.
ARTEMIS MMC	7.0	enabled	Enables MMC block within ARTEMIS library.
ARTEMIS MMC 2P	7.0	enabled	Enables ARTEMIS blockset with MMC 2P Block
ARTEMIS MMC CONTROLLER	7.0	enabled	Enables MMC controller block within ARTEMiS library.
ARTEMIS MMC FPGA	7.0	enabled	Enables multi-modular converter (MMC) models on FPGA
ARTEMIS NUM CORES	7.0	12 enabled	Number of activated core to execute a model in real-time with ARTEMIS library
ARTEMIS RT	70	enabled	Allows to execute models in real-time with ARTEMIS library
ARTEMIS RTF	70	enabled	Enables ARTEMIS blockset
ARTEMIS SSN	70	enabled	Enables ARTEMIS blockset with SSN option
RTE DRIVE NUM CORES	40	12 enabled	Number of activated core to execute a model in real-time with RT-EVENTS library
RTE DRIVE RT	40	enabled	Allows to execute models in real-time within RT-EVENTS
RTE NUM CORES	40	12 enabled	Number of activated core to execute a model in real-time with RT-EVENTS library
RTE RT	40	enabled	Allows to execute models in real-time within RT-EVENTS
OPIMAG RT	2.2	enabled	Enables OPIMAG blockset
BERTA RT	7.0	enabled	Enables Berta blockset
ETHERCAT SLAVE	11.0	enabled	Enables EtherCAT slave protocol ontion
IEC61850 GOOSE	20	enabled	Enables IEC61850 GOOSE protocol option
IEC61850 NUM CORES	20	12 enabled	Number of enabled threads for IEC61850 protocol
IEC61850 SAMPLED VALUES	20	enabled	Enables IEC61850 Sampled Values protocol option
IEC 60870 5 104 SLAVE	11.0	enabled	Enables IEC-60870-5-104 slave protocol option
IEEE1588 MASTER	11.0	enabled	Enables Master mode for the PTP module on the Spectracom TSync PCIe card
IEEE1588 SLAVE	11.0	enabled	Enables Slave mode for the DTD module on the Spectracom TSinc PCIe card
MODBUS SLAVE	11.0	enabled	Enables MODBLIS slave protocol ontion
	10	enabled	Enables ADBASOR im offline
	10	12 enabled	Number of anabled threads for the aDHASOPsim parallel feature
PHASOR RT	10	enabled	Enables ePHASORsim real-time
PICKERING	11.0	enabled	Enables Dickering driver ontion
PICKERINGEIL	11.0	enabled	Enables DickeringEll L driver option
RTYSG MMC	11.0	enabled	Enables RT_YSG blocket with MMC Block
SCODEVIEW	11.0	enabled	Enables the Scone//iew module for data analysis and chart reporting
SPECTRACOM	11.0	enabled	Enables GDS sunchronization with the Spectrosom TSure DCIe cord
YSG CONVERTER	11.0	enabled	Enables on a synchronization with the spectracom raying Pole card.
VSG DEV	11.0	enabled	Enables VSG development of custom firmware on EDGA
YSG EUS	11.0	enabled	Enables ultra-fact electric solver (eHS) on EPGA
	11.0	endbled	Enables encodes block set on EDGA
YSG ED	11.0	enabled	Enables VSG floating point (ED) block set on EDGA
VSG MMC CELLS DED VALVE	11.0	500 onabled	chables ASG floating point (PP) block set on PPGA
VEC NINC VALVES	11.0	12 on object	MMC Volver
ASG_MINC_VALVES	11.0	12 enabled	Maximum number of value controllars
ASG_MINIC_VALVE_CONTROLLERS	11.0	12 enabled	maximum number of valve controllers
X5G_MUTOK_KCP	11.0	enabled	Enables the FPGA firmware for rapid control prototyping (RCP) of electric drive controlle
Y20-bW2W2H	11.0	enabled	Enables spacial harmonic (SH) PMSM motor models on FPGA
XSG_PMSM_VDQ	11.0	enabled	Enables variable-DQ (VDQ) PMSM motor models on FPGA
XSG_RI	11.0	enabled	Enables XSG runtime execution of custom firmware on FPGA
	11.0	heldene	Enables EPGA signal display on a fast real-time oscilloscope
XSG_SCOPE	11.0	chabicu	chastes if a congrant applay of a fast rear time oscilloscope

Overview Diagnostic Simulation Settings Software License

Figure 12: Required licenses



BUILDING THE MODEL

- 1. In the Preparing and Compiling window, click **Build the model**. The Building Model window appears.
- 2. Verify that the model was successfully built by clicking **Consult result in Compilation View**.

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့ Overviev	w	<u>^</u>					
General Infor	mation	Preparing and Compiling					
Name:	Converter3Phase3LeveINPC_OP4510_rtlab	Edit the model.					
Path:	C:/Users/deniselefebvre/OPAL-RT/RT-LABv11_Workspace/eHS example/rtlab/Converter3Phase	Set the development properties.					
Matlab:	R2010B	Build the model.					
State:	Compiling	Consult result in the <u>Compilation View</u>					
Description:	Building model	Assign targets to subsystems.					
	Building Converter3Phase3LeveINPC_OP4510_rtlab Code compilation: skipped	roperties.					
	Always run in background	Details >> ples in the <u>Variables Table</u> .					

Figure 13: Building the model

💷 Display 🔲 Properties 📓 Compilation 🙁 📣 Matlab View 📮 Console 🔄 Variables T 🏢 Variable Vi 🐻 Monitoring 🖙						
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opicc -c -O2 -xHost -falign-functions=2 -diag-disable remark,warn,cpu-dispatch -DUSE_RTMODEL -DMODEL=	=0					
opicc -c -O2 -xHost -falign-functions=2 -diag-disable remark,warn,cpu-dispatch -DUSE_RTMODEL -DMODEL=	=C					
opicc -c -O2 -xHost -falign-functions=2 -diag-disable remark,warn,cpu-dispatch -DUSE_RTMODEL -DMODEL	*C					
opicc -c -02 -xHost -falign-functions=2 -diag-disable remark,warn,cpu-dispatch -DUSE_RTMODEL -DMODEL=	=C					
opicc -c -02 -xHost -falign-functions=2 -diag-disable remark,warn,cpu-dispatch -DUSE_RIMODEL -DMODEL=	=C					
### Linking						
opicpc -Wl,-rpath='/usr/opalrt/v11.0.1.390/common/bin' -Wl,'-rpath=/usr/opalrt/v11.0.1.390/common/bin/x32	21					
chmod a+x converter3phase3leve_1_sm_controller_						
<pre>### Created executable: converter3phase3leve_1_sm_controller_</pre>						
Building model total duration : 00h:00m:06s Completed successfully						
Transferring the built model						
Connecting to 192.168.10.77 OK.						
Transferring in binary mode /home/lenovo-seb/c/users/sebastiencense/opal-rt/rt-labv11_demos/ehs_example/mc						
Transferring in ascii mode /home/lenovo-seb/c/users/sebastiencense/opal-rt/rt-labv11_demos/ehs_example/moc						
File transfer duration : 00h:00m:02s						
completed successfully						
End at : Thursday, October 15, 2015, 09:42:36						
Compilation duration : 00h:01m:41s						
Updating status for next buildOK	-					
<	-					

Figure 14: Compilation view



3. Assign a target to the master subsystem simulation from the Subsystem Settings page. XHP must be **ON**.

SMyOP4510 Converter3Phase3LevelNPC_OP4510_rtlab 🕸	
Subsystem settings	<u>^</u>
Assignations	Target utilities
Subsystems	Clean target Set as embedded Clear embedded
Select subsystems to edit their properties:	
Name Assigned n Platform XHP SM_Controller_eHS_IOs MyOP4510 Redhat ☑ ON	=
1 subsystem selected : SM_Controller_eHS_IOs	
Edit settings for selected subsystems:	
Choose a physical node: MyOP4510	
Overview Development Execution Variables Files Assignation Diagnostic Hardware Simulation Tools	τ

Figure 15: Assigning targets



EXECUTION PROPERTIES

In the *Execution Properties* tab, you must set the real time simulation mode to Hardware Synchronized.

Click the arrow in the field next to *Real-time simulation mode* and select **Hardware synchronized** from the drop down menu.

Image: MyOP4510 Image: SlevelNPC_OP4510_rtiab ≅					
Execution Properties					
Real-Time Properties		Performance Properties			
Target platform:	Redhat	Enable detection of overruns			
Real-time simulation mode:	Hardware synchronized 🗸 🗸	Action to perform on overruns:	Continue •		
Real-time communication link type	Simulation	Perform action after N overruns:	10		
Time Factor:	Software synchronized	Number of steps without overruns:	10		
Stop Time [s]:	Hardware synchronized				
Pause Time [s]:	Infinity •				
Overview Development Execution Variables Files Assignation Diagnostic Hardware Simulation Tools					

Figure 16: Execution properties window



LOADING THE MODEL

In the Overview tab, click on <u>Load</u> the model. The console will open, and the real-time code will be uploaded to the simulator. The Loading model window appears briefly during the loading process.

The **Display** tab in the lower portion of the window will show load progress and details.

😻 RT-LAB				
File Edit Navigate Search Simulation Run Tools Window Help				
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MyOP4510 Bell Sexample Models Converter3Phase3LeveINPC_OF Create a new project Loading model Loading Converter3Phase3Level	General Information Name: Converter3Phase3LeveINPC_OP4510_rtlab Path: C:/Users/deniselefebvre/OPAL-RT/RT-LABv11_Workspace/eHS exai Matlab: R20108 State: Loading NPC_OP4510_rtlab	Preparing and Compiling Image: Edit the model. Image: Setthe development properties. Image: Build the model. Image: Consult result in the Compilation View Image: Assign targets to subsystems. Executing Image: Set the execution properties. Image: Load the model.		
Always run in background	un in Background Cancel Details >> v I Console Vari			
<pre>Transferring in binary: C:\Users\deniselefebvre\OPAL-RT\RT-LABv11_Workspace\eHS example\rtlab\Converter3Phase3I Transferring in binary: C:\Users\deniselefebvre\OPAL-RT\RT-LABv11_Workspace\eHS example\rtlab\ED741_3-EX-0001 Transferring in binary: C:\Users\deniselefebvre\OPAL-RT\RT-LABv11_Workspace\eHS example\rtlab\Converter3Phase3I Transferring in binary: C:\</pre>				
		🛃 Loading model 🛛 🛶 👘		

Figure 17: Loading model window



EXECUTING THE SIMULATION

Click on **Execute the model** to start the simulation. At the beginning of the simulation, eHS will initialize (it takes about 10,000 simulation steps). During this time the eHS outputs will remain at 0.

Clicking on the **Display** tab shows execution details.

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Tools Window Help					
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■ MyOP4510 ■ localhost ■ Converter3Phase3LevelNPC_OP4510_rtlab 🖾					
Matlab: R2010B	Build the model.				
State: Dupping	Consult result in the Compilation View				
Description:	Assign targets to subsystems.				
	Executing				
	Set the execution properties.				
	Load the model.				
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	in the <u>Variables Table</u> .				
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Converter3Phase31					
Real-time Singuetasking mode.					
KT-LAB LICENSE OK. 3// OAYS FEMENINING. Snapshot taken (opconverter3phase3leve sm controller 0.snap).					
[0]: PAUSE mode, IO set to pause value.					
Mon Feb 8 10:32:57 2016					
Starting transfer of /home/laptop-denise/c/users/denise/repute/opal-t/rt-labv1_workspace/ess example/rtlab/converter3phase3levelnpc <					
XHP mode enabled					
Synchronized step size = 25 us.					
Mon Feb 8 10:34:27 2016					
Open file done (/./myfile.mat)					
Main priority set to 99					
	🔏 Running Console 🛛 🔤 🐿				

Figure 18: Displaying execution details



MONITORING THE SIMULATION

As soon as you load and execute the model, the Simulink console opens (behind RT-LAB) and you should be able to see the simulation running in the console window. The following example shows the three-phase load current of the converter.



Figure 19: Console window of running model



Figure 20: Displaying signals in the Simulink console



CONTROLLING THE SIMULATION

Simulation operating conditions can be modified directly from the console. Simply click the desired signal in the console to open its *Block Parameters* window.



Figure 21: Changing parameter values in the console





Figure 22: Impact of changing parameter values

CONTACT

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