EHS QUICKSTART GUIDE

eFPGAsim Toolbox

RTLAB / CPU Section

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Contents

INTRODUCTION

The eHS solver is an FPGA-based technology developed by OPAL-RT for real-time power electronics simulation. Thanks to a convenient circuit schematic graphical user interface, the FPGA code is automatically generated, making FPGA-based simulation accessible to a large number of users.

This document provides basic information on how to create a new project with a template that includes the eHS solver and how to run a real-time simulation with an example model included in the template. The guide is designed for the OP45xx and OP56xx targets.

REQUIREMENTS

OPAL-RT HARDWARE

- OP4500 / OP4510 / OP4520
- OP5607 / OP5600 / OP5707

RECOMMENDED OPERATING SYSTEM

Microsoft Windows 7 64bits Version 6.1 (Build 7601: Service Pack 1)

PRE-INSTALLED SOFTWARE

The following software must be installed and functioning to perform the tests described in this document. Confirm that the required software is installed and test to ensure they are functioning properly.

Type >> *ver* on the MATLAB prompt and verify that you have the following toolboxes (or later versions of them) installed.

Recommended configurations for basic use (only circuit simulation):

- MATLAB 2011b / 2013a / 2015aSP1, 32-bit version
- RT-LAB v11.1.3 or later
- At least one of the following tools:
    - SimPowerSystems “Specialized Technology” Simulink library
    - Powersim PSIM v9.3.4 or v10.0.6 (v10.0.5 is unsupported)
    - Plexim PLECS Simulink Library v3.7.4
    - NI Multisim 13

The RT-XSG toolbox requires the following software to generate programming files for reconfigurable devices and to program the platform:

Recommended configuration for firmware generation, for Xilinx 7 series:

- MATLAB 2015b, 64-bit version
- Xilinx Vivado suite 2015.3 & Xilinx Vivado System Generator for DSP 2015.3
- RT-XSG v3.1.2 or later

LICENSED RT-LAB COMPONENTS

You must have licenses for the following RT-LAB components to run the examples provided in this document. Verify with your sales representative that your system includes these licenses.

RTLAB_RT	RTLAB_XHP	RTLAB_DEV	RTLAB_NUM_CORES >= 1
RTE_RT	RTE_NUM_CORES >= 1	XSG_EHS	

RUNNING A MODEL ON OP45XX/OP56XX TARGETS

CREATING A NEW RT-LAB PROJECT

Open RT-LAB and follow these steps to create a new RT-LAB project:

1. In the main RT-LAB User Interface, navigate to **File > New > RT-LAB Project** to open a new project wizard.
2. Enter a project name (e.g. *eHS_examples*), then click **Next**.
3. Browse the template directory to select the model to add it to the project. Open the *eFPGAsim* folder and select **eHS with IOs > OP4510 > eHSx64_with_IOs_on_OP4510 (Simulink).**
4. Click **Finish** to create the new RT-LAB project in the project explorer.

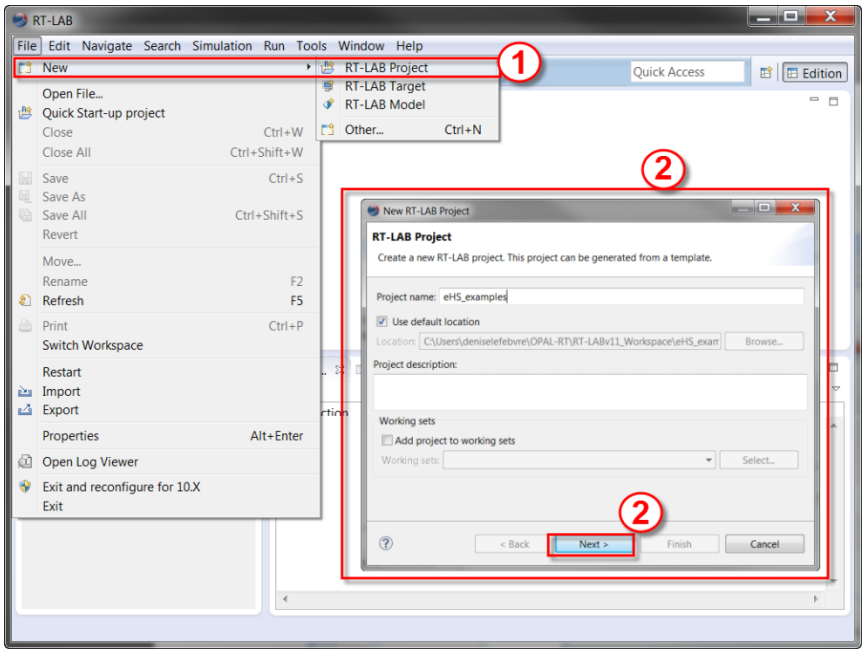


Figure 1: Creating a new project

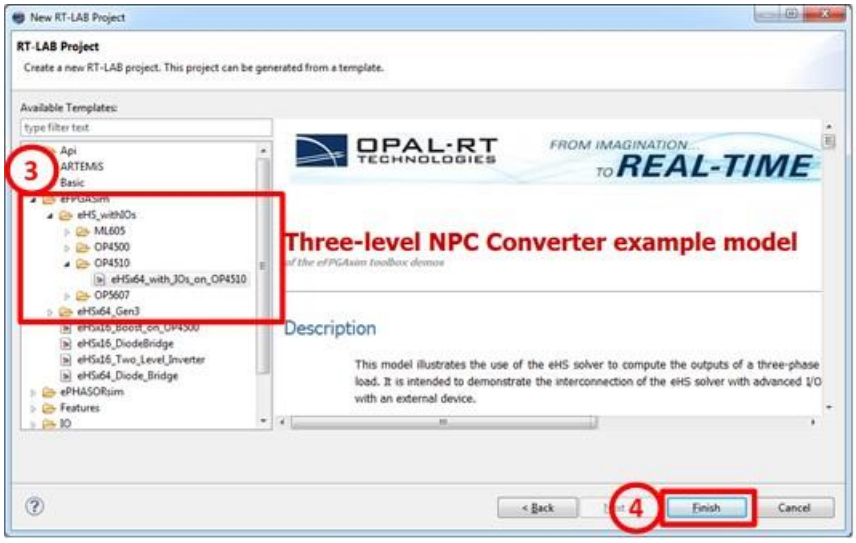


Figure 2: Browsing model templates

The *eHS_examples* project will be created and the corresponding RT-LAB model will be imported into the project workspace (in this example, the model is named *Converter3Phase3LevelNPC_OP4510_rtlab*).

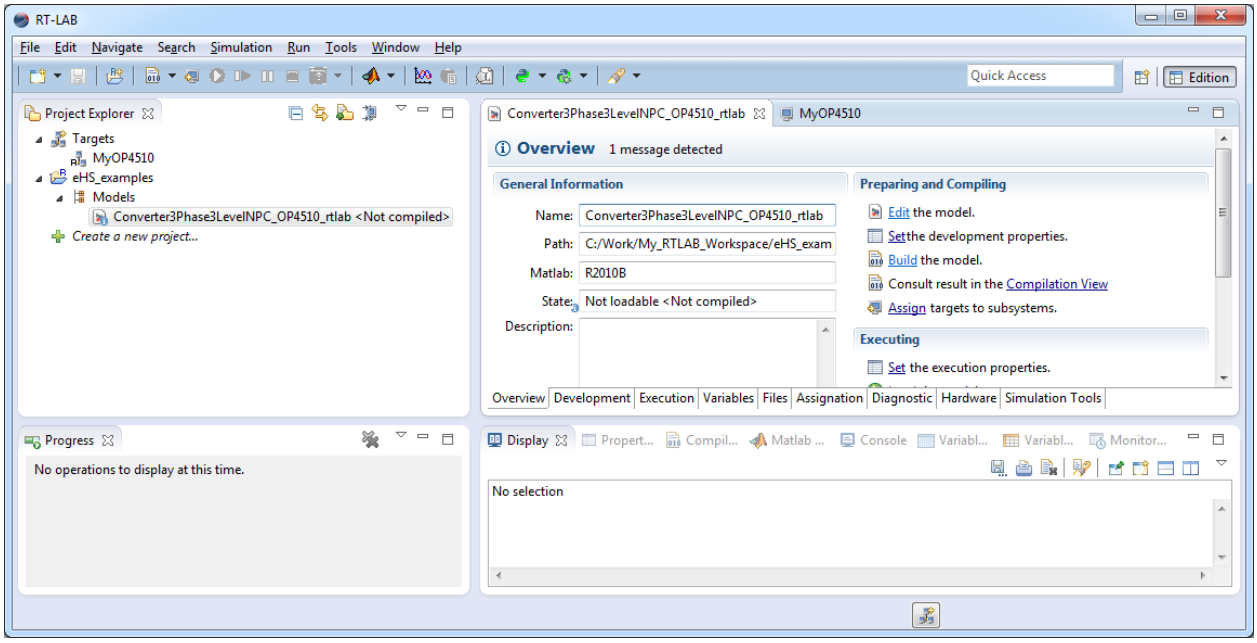


Figure 3: Example workspace

EDITING THE MODEL

Before building the model, verify that you can access and edit the model.

Click on **Edit the model** in the *Preparing and Compiling* pane. The model file will be opened in a new MATLAB/Simulink window.

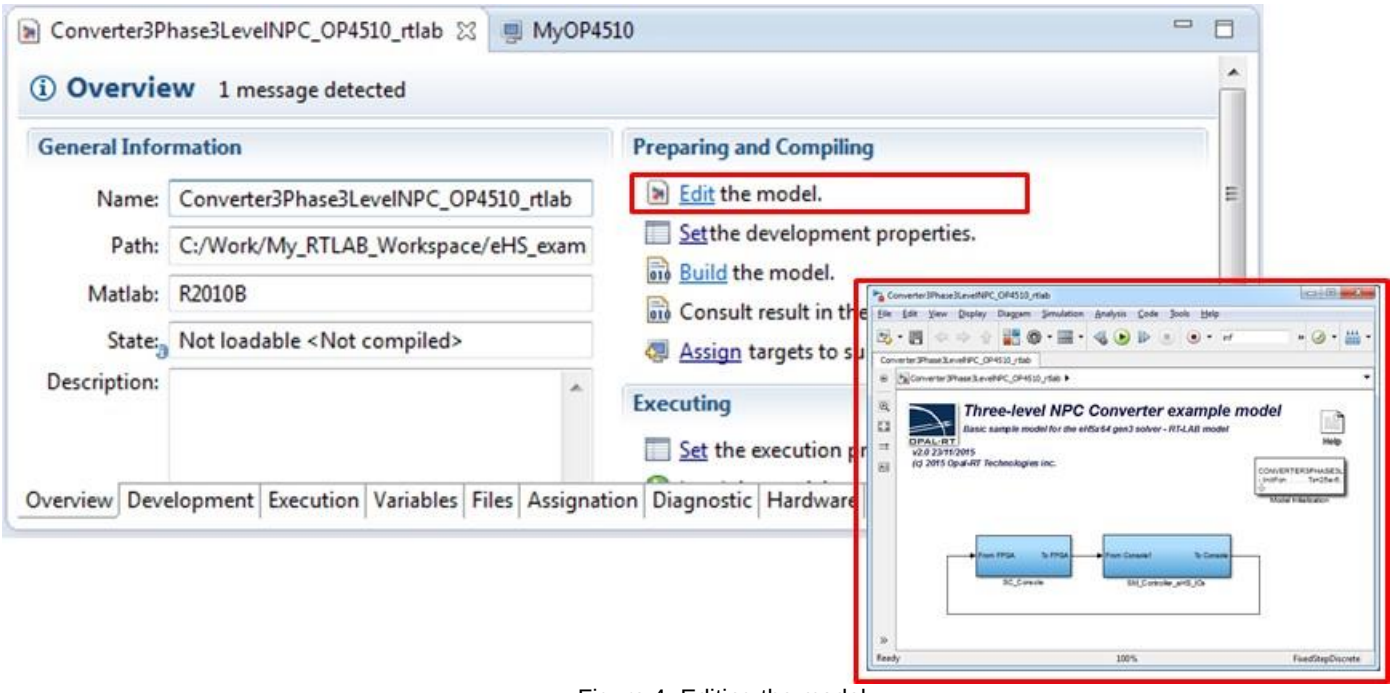


Figure 4: Editing the model

MODEL DESCRIPTION

The model is composed of two main subsystems:

1. *SC_Console*: Subsystem executed by the host computer during the simulation to monitor and control the simulation.
2. *SM_Controller_eHS_IOs*: Subsystem executed by the target simulator, in real-time, on the system CPU that communicates with the FPGA board and the physical system I/Os.

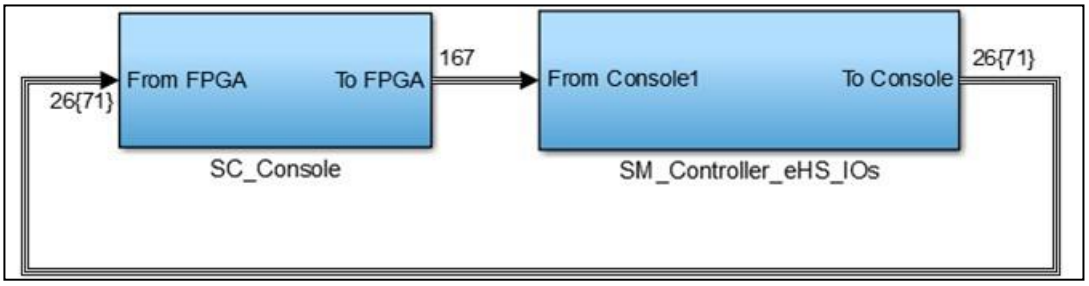


Figure 5: Model diagram

SC_CONSOLE

Double click on the **SC_Console** to open the SC_Console details window.

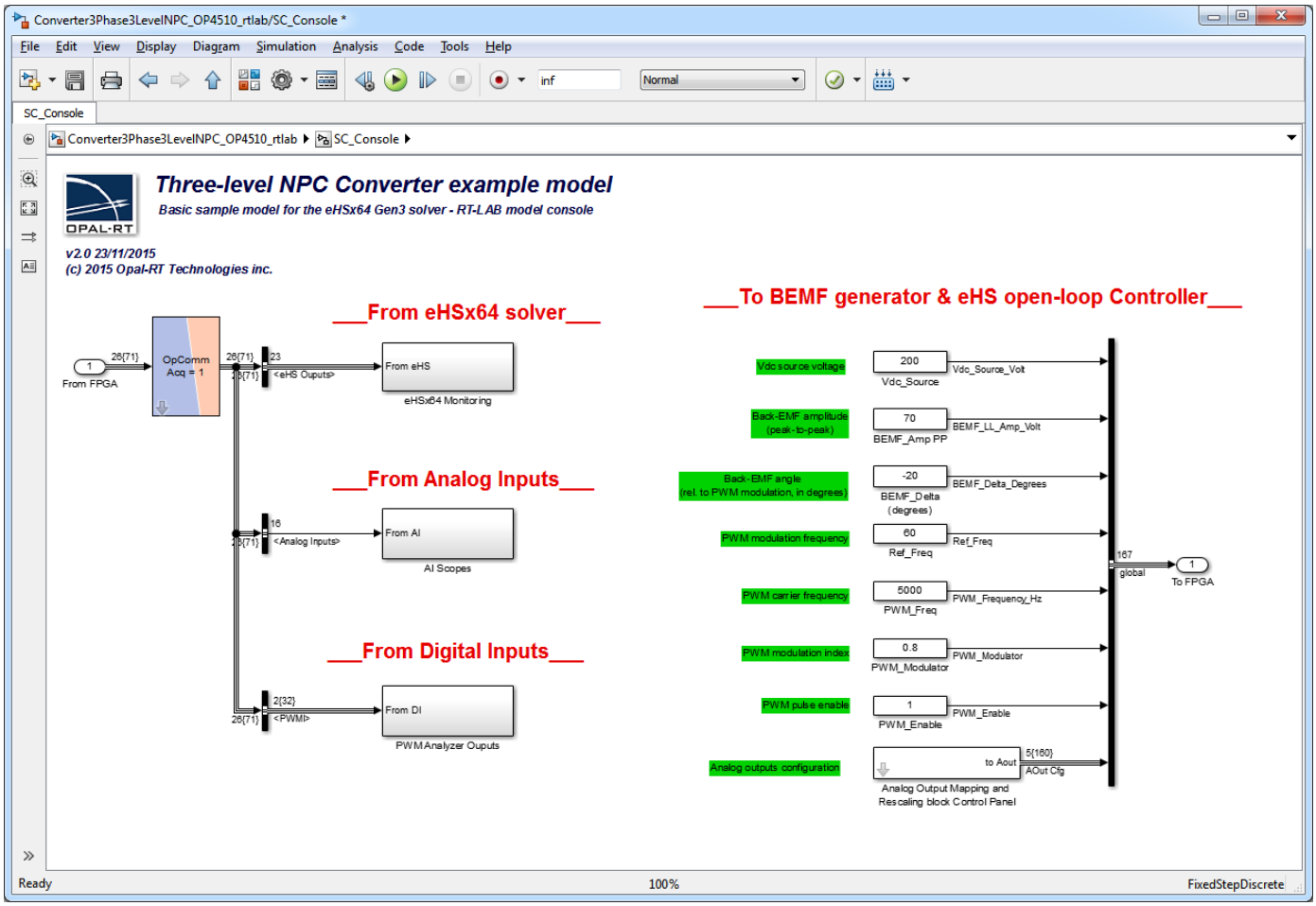


Figure 6: Model SC_Console window

SM_CONTROLLER_EHS_IOS

Click on the **SM_Controller_eHS_IOs** to open the SM details window. This window provides a detailed diagram of the master subsystem.

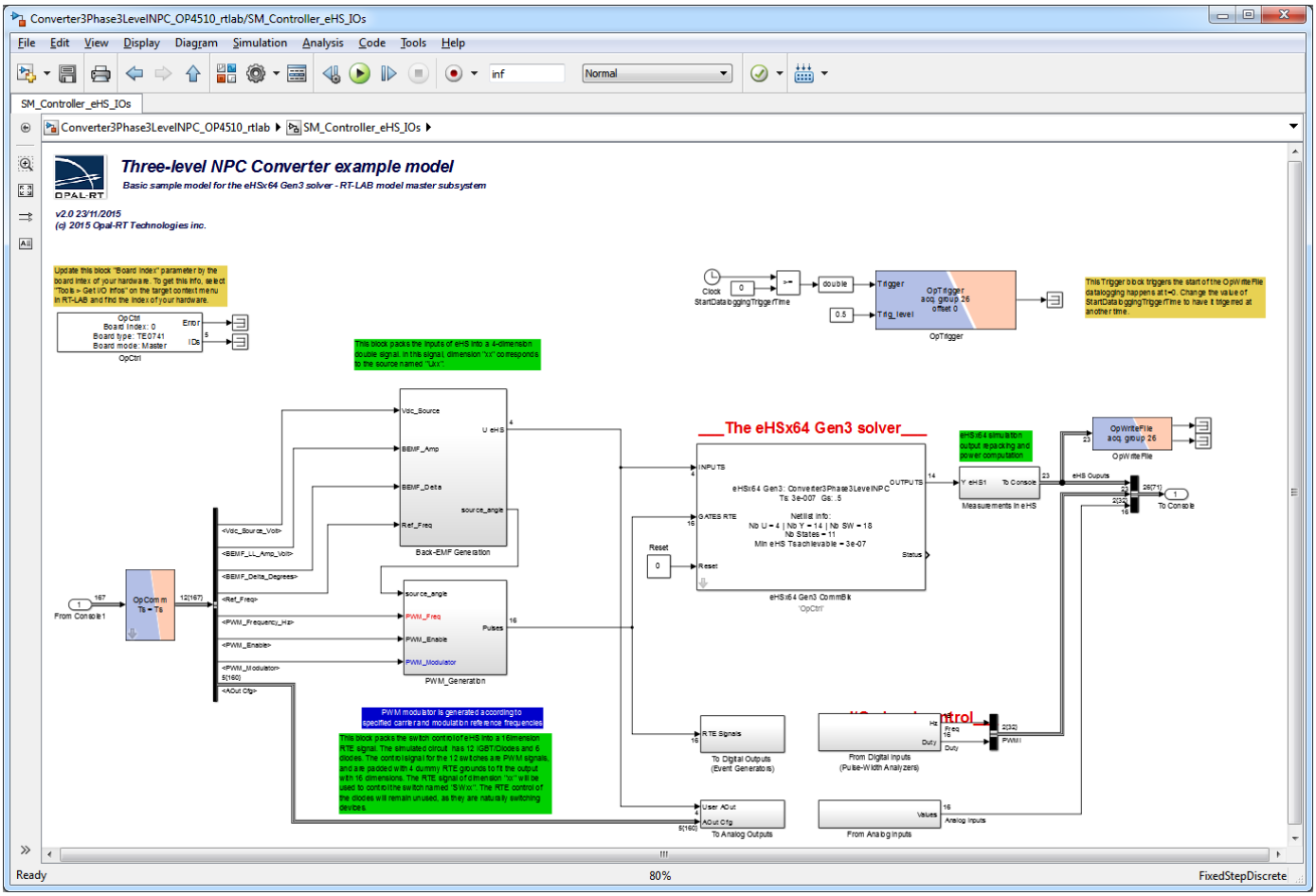


Figure 7: Model SM_Controller_eHS_IOs window

EHS GEN3 COMMBLK

The *eHS Gen3 CommBlk* communicates with the FPGA board to initialize the eHS core. During real-time operation, it provides eHS inputs (the circuit Sources / Gates control signals) and reads the eHS outputs (current and voltage measurements) at the RT-LAB model rate.

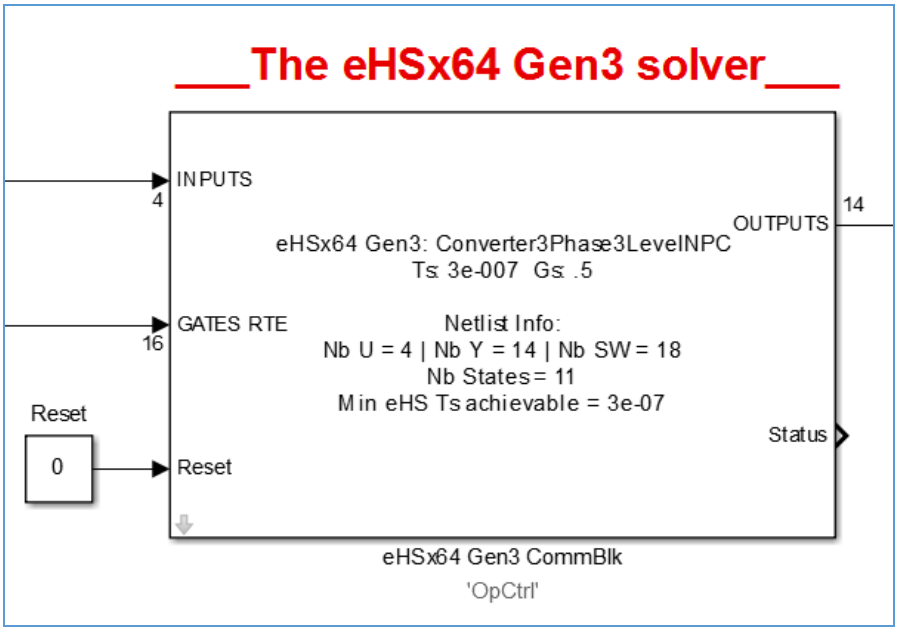


Figure 8: eHSx64 Gen3 CommBlk diagram

The user must provide a circuit file (SimPowerSystems Simulink model, PSIM file, PLECS Simulink model, or NI Multisim 13 XML netlist) to declare the circuit that will be simulated inside the eHS core.

In this example, the circuit file is a SimPowerSystems Simulink model named *Converter3Phase3LevelNPC.mdl*.

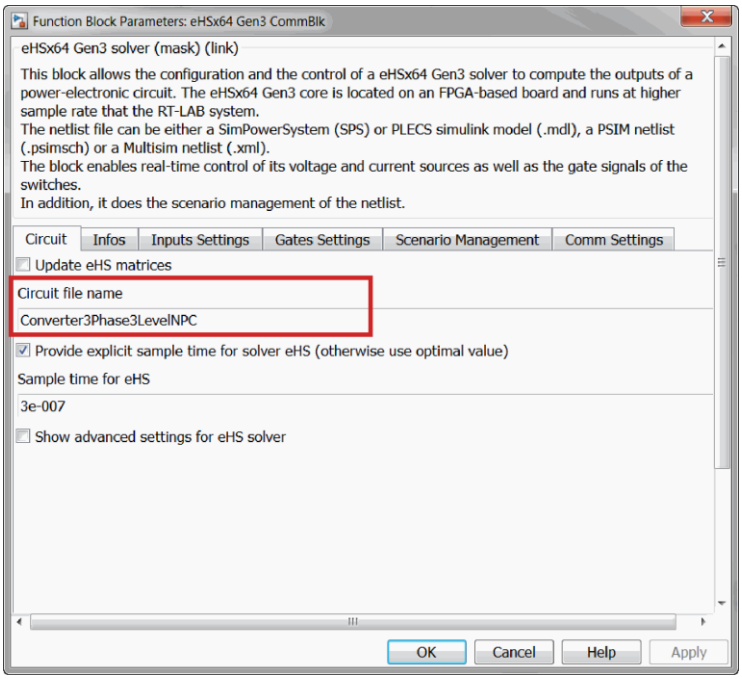


Figure 9: Block parameters window

CIRCUIT FILE

The circuit file models an NPC converter. The eHS solver will extract the components netlist from this file and calculate the system equations before running them on the FPGA board.

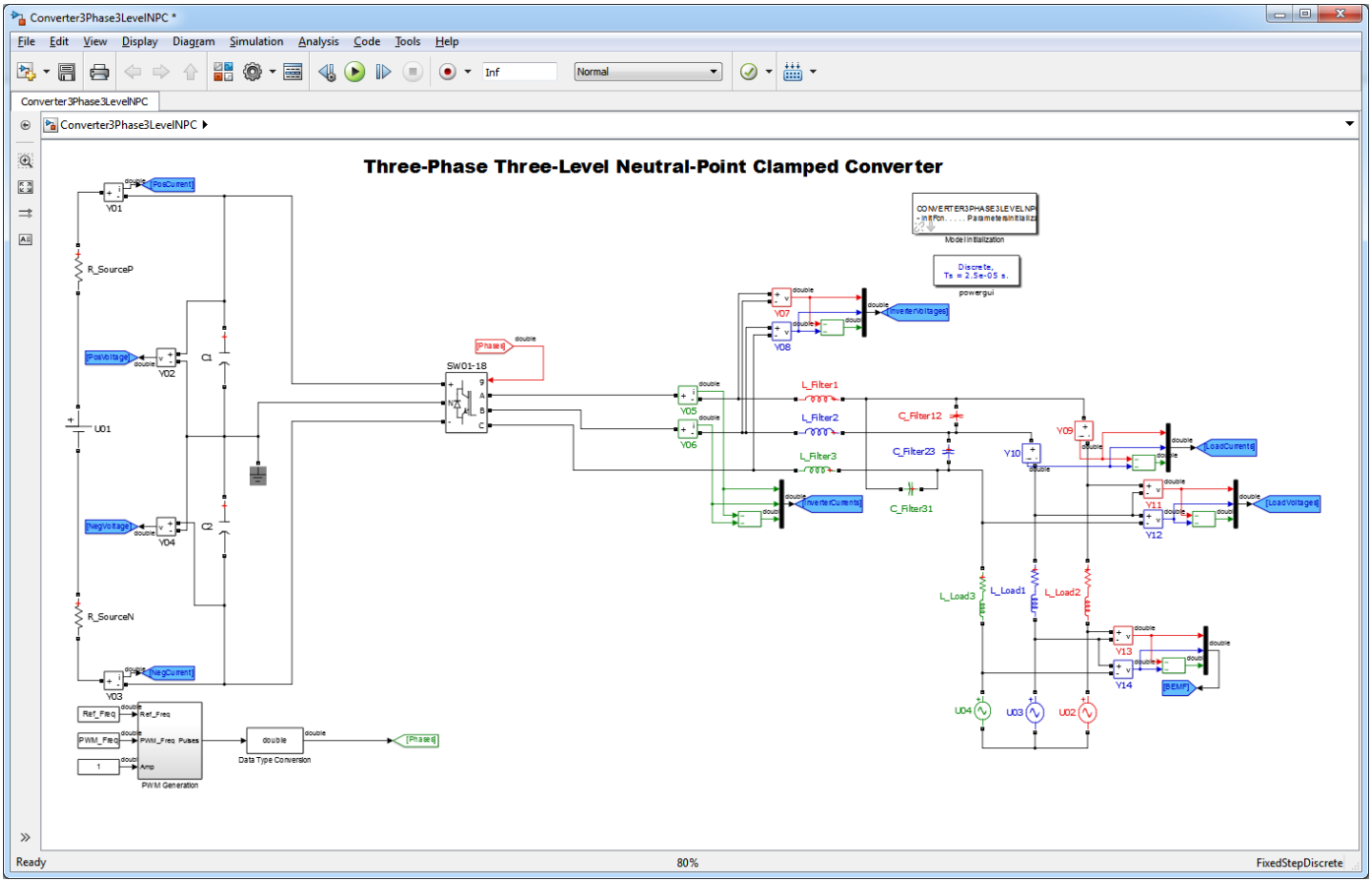


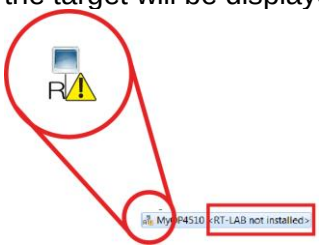
Figure 10: Model converter diagram

VALIDATING THE MODEL

Run an offline simulation from the RT-LAB model to ensure that all the library links are resolved using your MATLAB instance.

Verify that the model runs properly.

- In RT-LAB, check that your target is available in the Targets list, and is up and running (any problems with the target will be displayed by RT-LAB as an icon change and added text after the target name).



- Right-click your target and select **Set as development node**

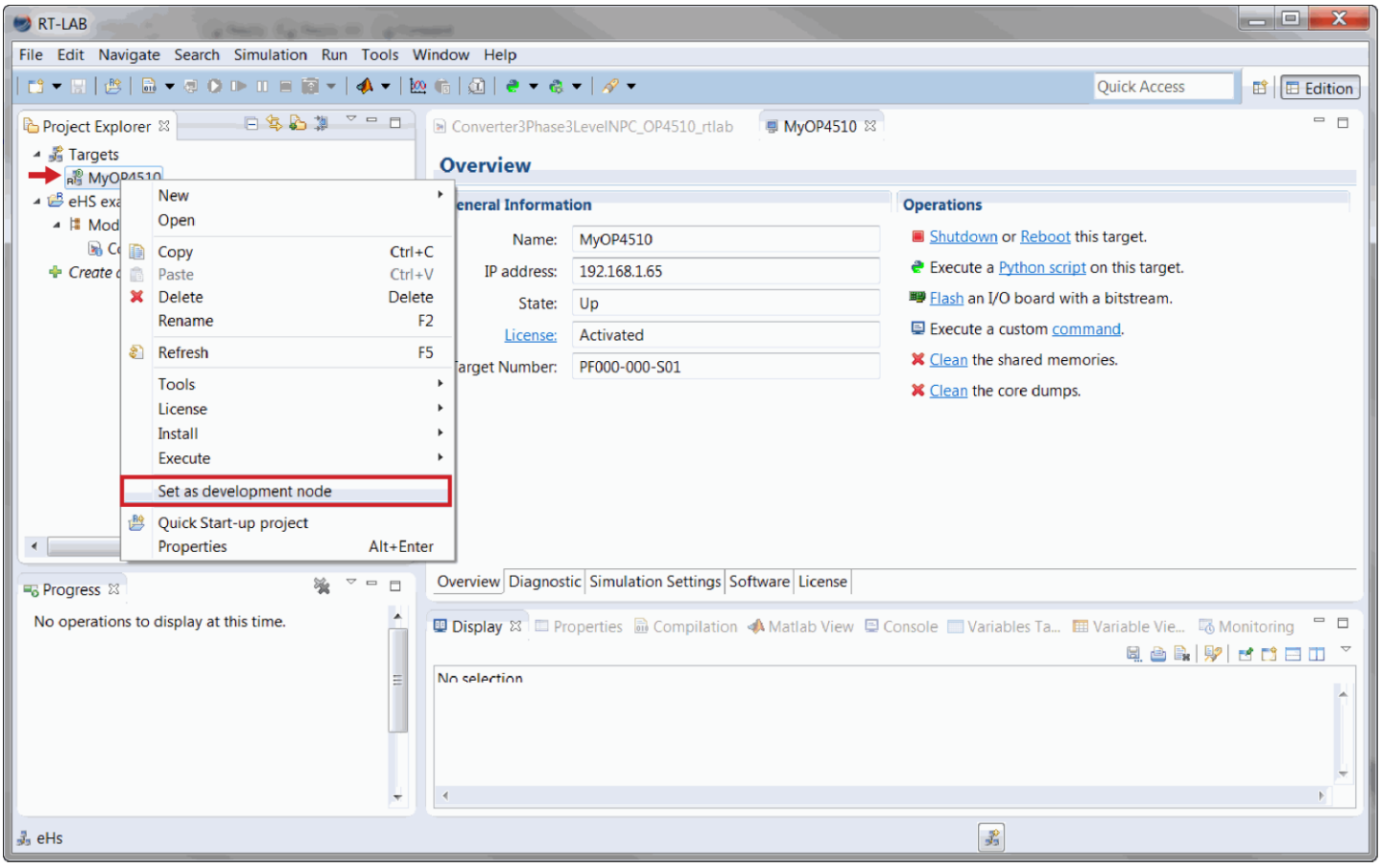


Figure 11: Setting the target as development node

- Click on the **License** tab to display the list of software licenses and make sure that XSG_EHS, RTLAB_RT, RTLAB_DEV, RTLAB_XHP and RTE_RT licenses are enabled. You must also have at least RTLAB_NUM_CORES and RTE_NUM_CORES >= 1.

Feature name	Version	Status	Description
RTLAB_NRT	11.0	enabled	Allows to execute a model in non real-time mode
RTLAB_NUM_CORES	11.0	12 enabled	Allows to execute a model in non real-time mode with RT-LAB.
RTLAB_RT	11.0	enabled	Allows to execute a model in real-time mode with RT-LAB.
RTLAB_XHP	11.0	enabled	Enables the XHP mode within RT-LAB.
RTLAB_ARINC429	11.0	enabled	Enables ARINC429 protocol option.
RTLAB_C37_118_MASTER	11.0	enabled	Enables C37.118 master protocol option.
RTLAB_C37_118_SLAVE	11.0	enabled	Enables slave Synchrophasor Protocol C37.118.
RTLAB_COMM_FW	11.0	enabled	Enables to distribute simulation over a cluster of target using Firewire realtime link.
RTLAB_COMM_SCI	11.0	enabled	Enables to distribute simulation over a cluster of target using Dolphin realtime link.
RTLAB_DEV	11.0	enabled	Allows to compile a model.
RTLAB_DNP3_SLAVE	11.0	enabled	Enables slave Distributed Network Protocol (DNP3).
RTLAB_FIELDBUS	11.0	enabled	RTLAB_FIELDBUS
RTLAB_IO_61850	11.0	enabled	Enables IEC61850 communication protocol for protection relay interface.
RTLAB_KETEREX_I2C	11.0	enabled	Enables Keterex I2C communication protocol.
RTLAB_KETEREX_SPI	11.0	enabled	Enables Keterex SPI communication protocol.
RTLAB_OPC	11.0	enabled	Enables Open Platform Communications (OPC) protocol.
RTLAB_ORCHESTRA	11.0	enabled	Enables Orchestra co-simulation framework.
RTLAB_SPECTRACOM_TSYNC_PCIE	11.0	enabled	Enables GPS synchronization with the Spectracom TSync PCIe card.
ARTEMIS_MMC	7.0	enabled	Enables MMC block within ARTEMiS library.
ARTEMIS_MMC_2P	7.0	enabled	Enables ARTEMIS blockset with MMC 2P Block
ARTEMIS_MMC_CONTROLLER	7.0	enabled	Enables MMC controller block within ARTEMiS library.
ARTEMIS_MMC_FPGA	7.0	enabled	Enables multi-modular converter (MMC) models on FPGA
ARTEMIS_NUM_CORES	7.0	12 enabled	Number of activated core to execute a model in real-time with ARTEMiS library.
ARTEMIS_RT	7.0	enabled	Allows to execute models in real-time with ARTEMIS library.
ARTEMIS_RTE	7.0	enabled	Enables ARTEMIS blockset.
ARTEMIS_SSN	7.0	enabled	Enables ARTEMIS blockset with SSN option.
RTE_DRIVE_NUM_CORES	4.0	12 enabled	Number of activated core to execute a model in real-time with RT-EVENTS library.
RTE_DRIVE_RT	4.0	enabled	Allows to execute models in real-time within RT-EVENTS
RTE_NUM_CORES	4.0	12 enabled	Number of activated core to execute a model in real-time with RT-EVENTS library.
RTE_RT	4.0	enabled	Allows to execute models in real-time within RT-EVENTS.
OPJMAG_RT	2.2	enabled	Enables OPJMAG blockset.
BERTA_RT	7.0	enabled	Enables Berta blockset
ETHERCAT_SLAVE	11.0	enabled	Enables EtherCAT slave protocol option.
IEC61850_GOOSE	2.0	enabled	Enables IEC61850 GOOSE protocol option.
IEC61850_NUM_CORES	2.0	12 enabled	Number of enabled threads for IEC61850 protocol.
IEC61850_SAMPLED_VALUES	2.0	enabled	Enables IEC61850 Sampled Values protocol option.
IEC_60870_5_104_SLAVE	11.0	enabled	Enables IEC-60870-5-104 slave protocol option.
IEEE1588_MASTER	11.0	enabled	Enables Master mode for the PTP module on the Spectracom TSync PCIe card.
IEEE1588_SLAVE	11.0	enabled	Enables Slave mode for the PTP module on the Spectracom TSync PCIe card.
MODBUS_SLAVE	11.0	enabled	Enables MODBUS slave protocol option.
PHASOR_NRT	1.0	enabled	Enables ePHASORsim offline
PHASOR_PARALLEL	1.0	12 enabled	Number of enabled threads for the ePHASORsim parallel feature
PHASOR_RT	1.0	enabled	Enables ePHASORsim real-time
PICKERING	11.0	enabled	Enables Pickering driver option
PICKERINGFIU	11.0	enabled	Enables PickeringFIU driver option
RTXSG_MMC	11.0	enabled	Enables RT-XSG blockset with MMC Block
SCOPEVIEW	11.0	enabled	Enables the ScopeView module for data analysis and chart reporting.
SPECTRACOM	11.0	enabled	Enables GPS synchronization with the Spectracom TSync PCIe card.
XSG_CONVERTER	11.0	enabled	Enables converter block set on FPGA
XSG_DEV	11.0	enabled	Enables XSG development of custom firmware on FPGA
XSG_EHS	11.0	enabled	Enables ultra-fast electric solver (eHS) on FPGA
XSG_ENCODER	11.0	enabled	Enables encoder block set on FPGA
XSG_FP	11.0	enabled	Enables XSG floating point (FP) block set on FPGA
XSG_MMC_CELLS_PER_VALVE	11.0	500 enabled	MMC cells per valve
XSG_MMC_VALVES	11.0	12 enabled	MMC Valves
XSG_MMC_VALVE_CONTROLLERS	11.0	12 enabled	Maximum number of valve controllers
XSG_MOTOR_RCP	11.0	enabled	Enables the FPGA firmware for rapid control prototyping (RCP) of electric drive controller
XSG_PMSM_SH	11.0	enabled	Enables spacial harmonic (SH) PMSM motor models on FPGA
XSG_PMSM_VDQ	11.0	enabled	Enables variable-DQ (VDQ) PMSM motor models on FPGA
XSG_RT	11.0	enabled	Enables XSG runtime execution of custom firmware on FPGA
XSG_SCOPE	11.0	enabled	Enables FPGA signal display on a fast real-time oscilloscope
XSG_SRM	11.0	enabled	Enables switched reluctance motor (SRM) models on FPGA

Figure 12: Required licenses

BUILDING THE MODEL

1. In the *Preparing and Compiling* window, click **Build the model**. The *Building Model* window appears.
2. Verify that the model was successfully built by clicking **Consult result in Compilation View**.

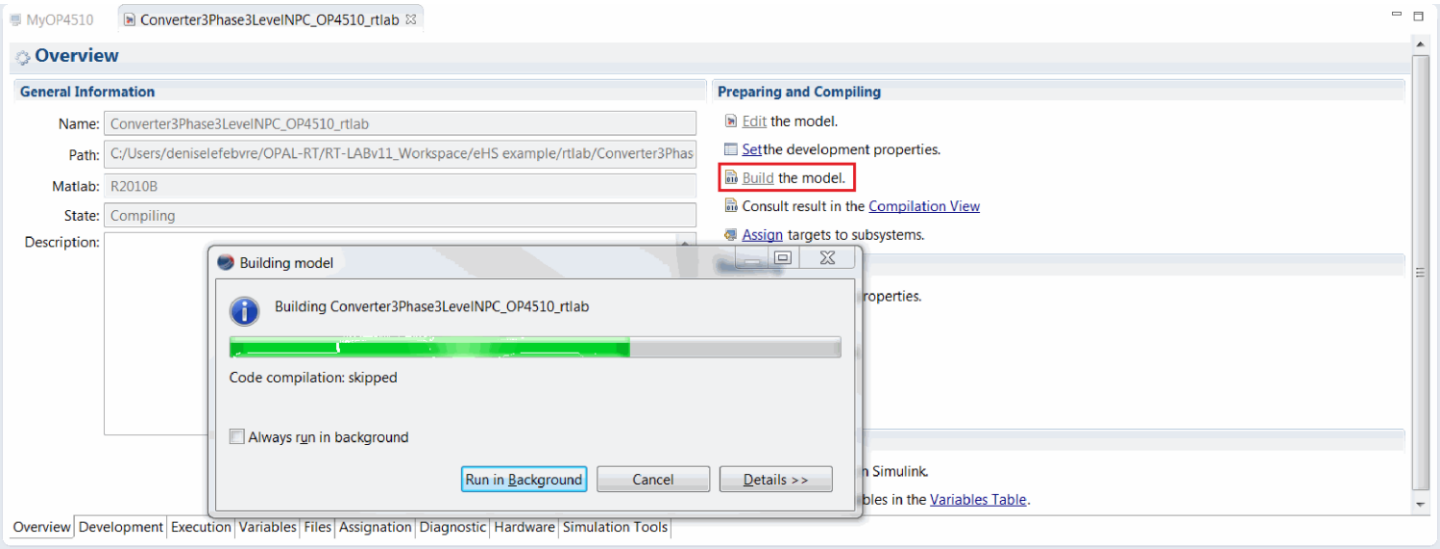


Figure 13: Building the model

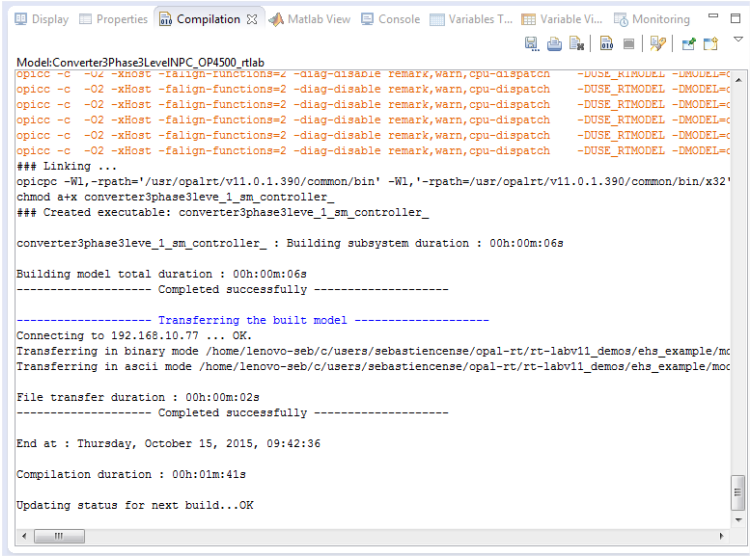


Figure 14: Compilation view

3. Assign a target to the master subsystem simulation from the Subsystem Settings page. XHP must be **ON**.

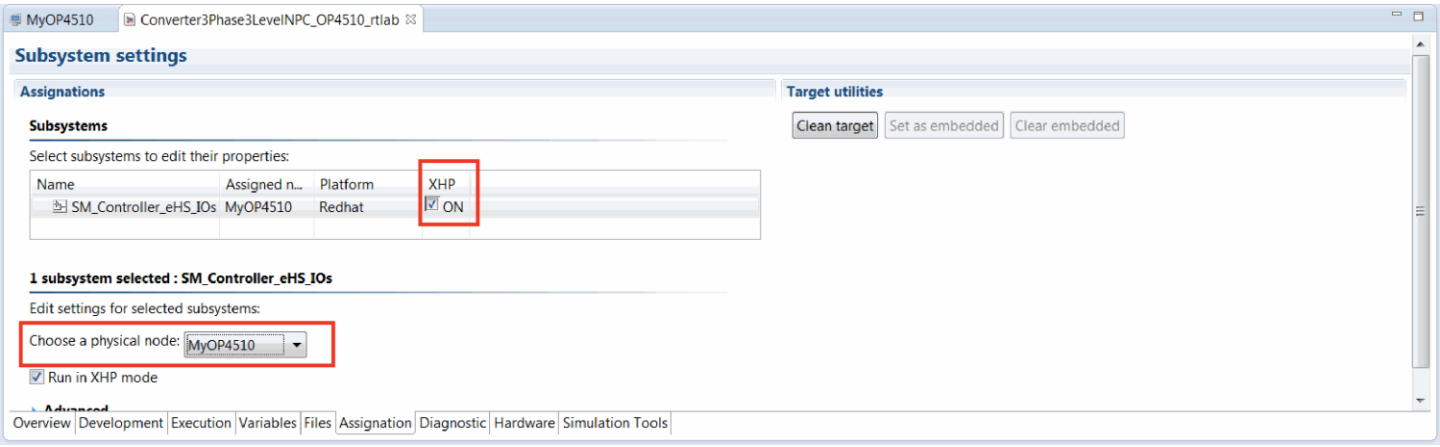


Figure 15: Assigning targets

EXECUTION PROPERTIES

In the *Execution Properties* tab, you must set the real time simulation mode to **Hardware Synchronized**.

Click the arrow in the field next to *Real-time simulation mode* and select **Hardware synchronized** from the drop down menu.

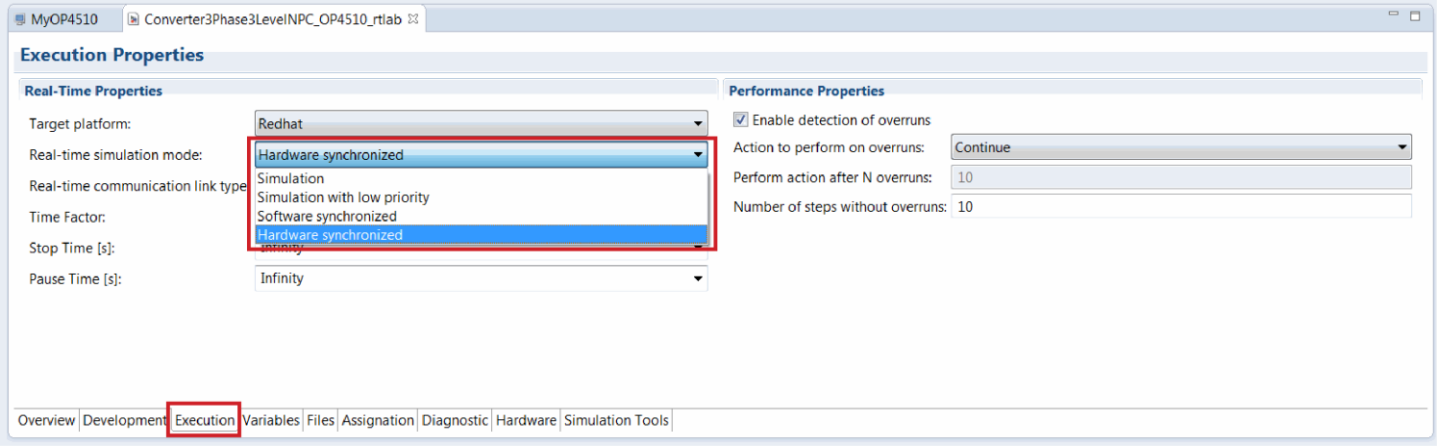


Figure 16: Execution properties window

LOADING THE MODEL

In the Overview tab, click on **Load the model**. The console will open, and the real-time code will be uploaded to the simulator. The **Loading model** window appears briefly during the loading process.

The **Display** tab in the lower portion of the window will show load progress and details.

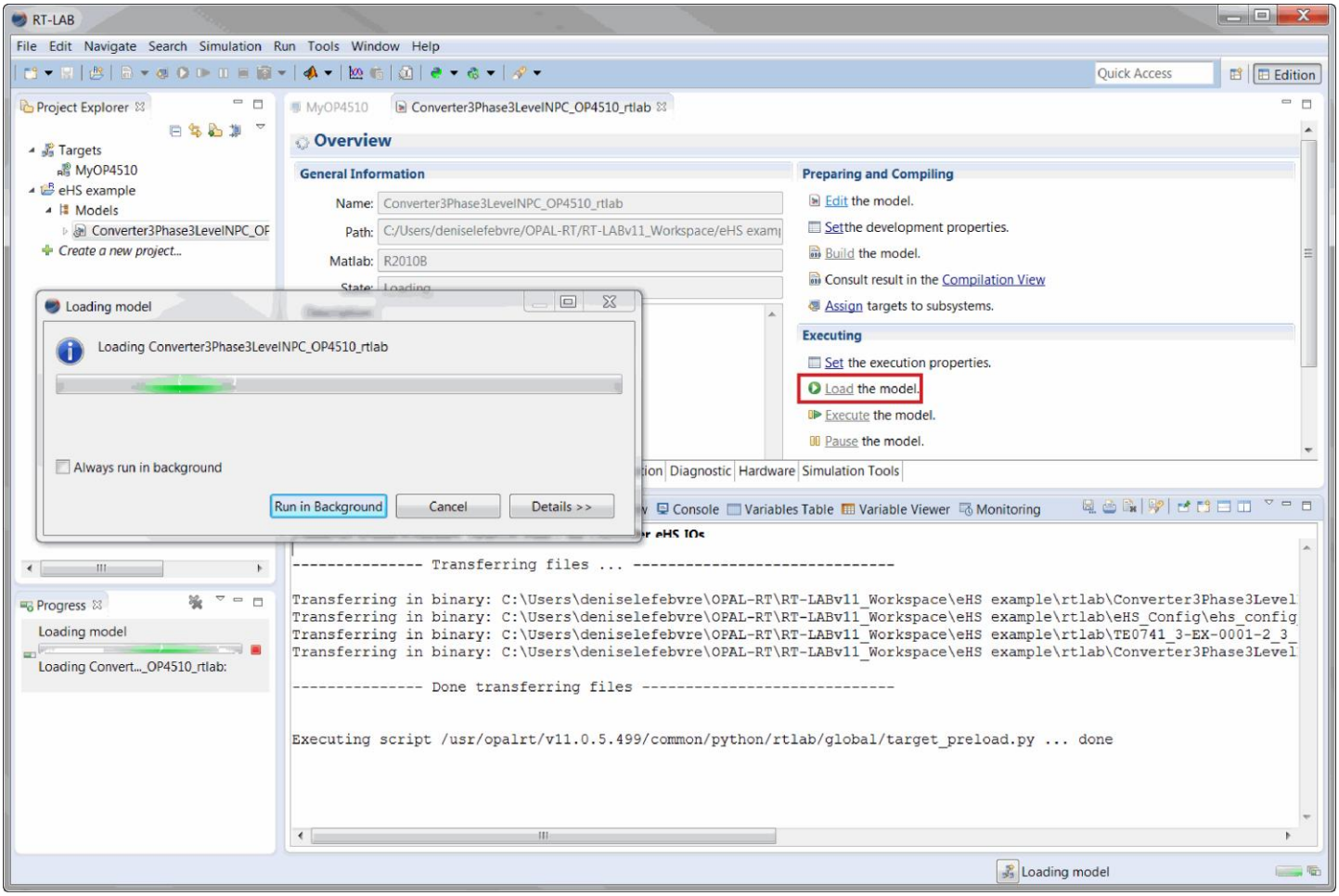


Figure 17: Loading model window

EXECUTING THE SIMULATION

Click on **Execute** **the model** to start the simulation. At the beginning of the simulation, eHS will initialize (it takes about 10,000 simulation steps). During this time the eHS outputs will remain at 0.

Clicking on the **Display** tab shows execution details.

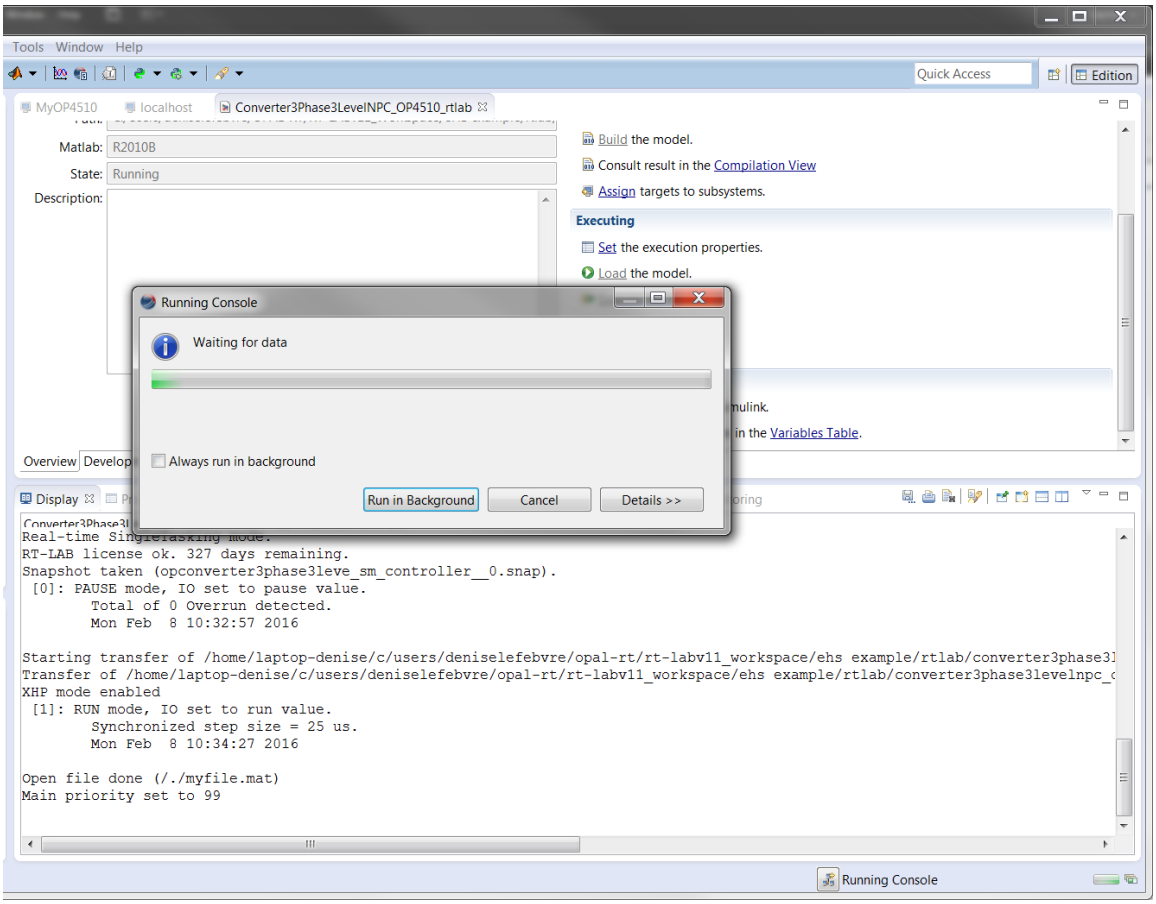


Figure 18: Displaying execution details

MONITORING THE SIMULATION

As soon as you load and execute the model, the Simulink console opens (behind RT-LAB) and you should be able to see the simulation running in the console window. The following example shows the three-phase load current of the converter.

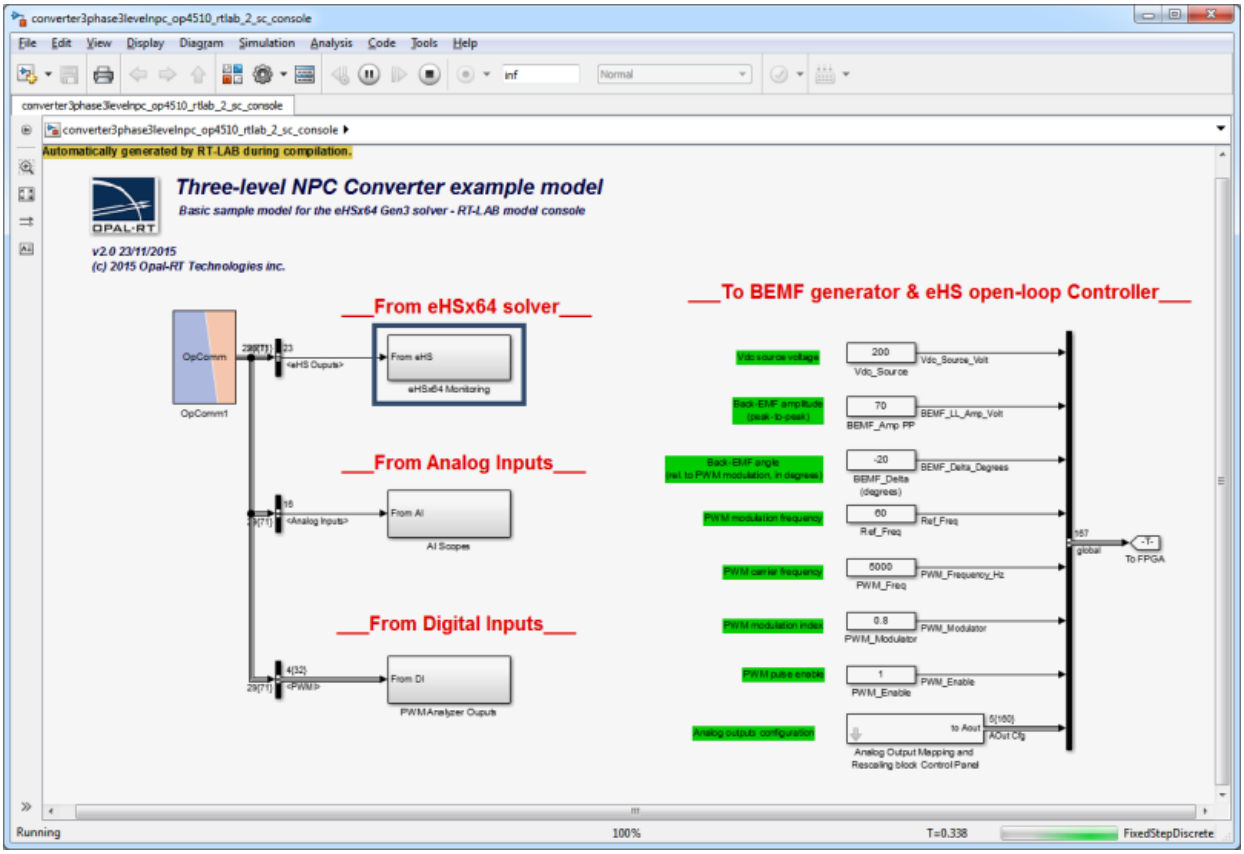


Figure 19: Console window of running model

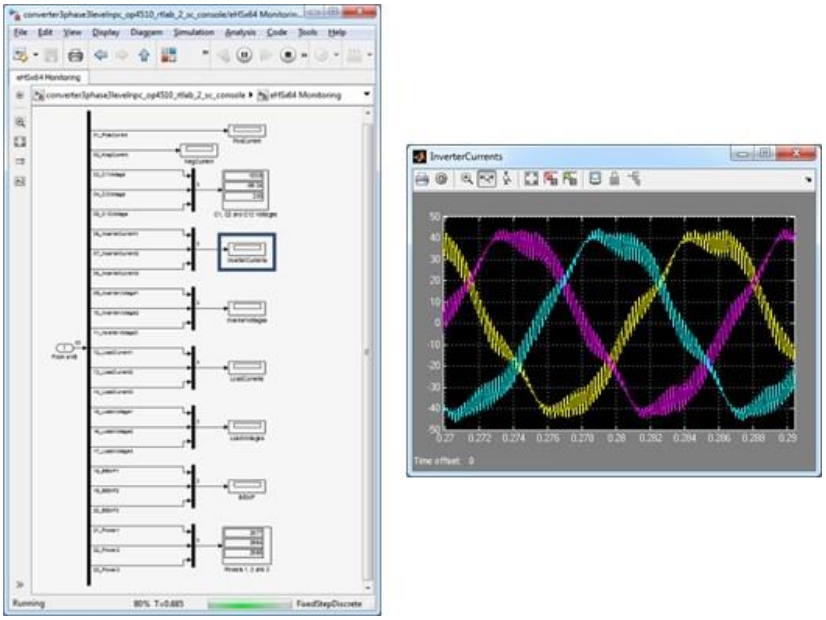


Figure 20: Displaying signals in the Simulink console

CONTROLLING THE SIMULATION

Simulation operating conditions can be modified directly from the console. Simply click the desired signal in the console to open its *Block Parameters* window.

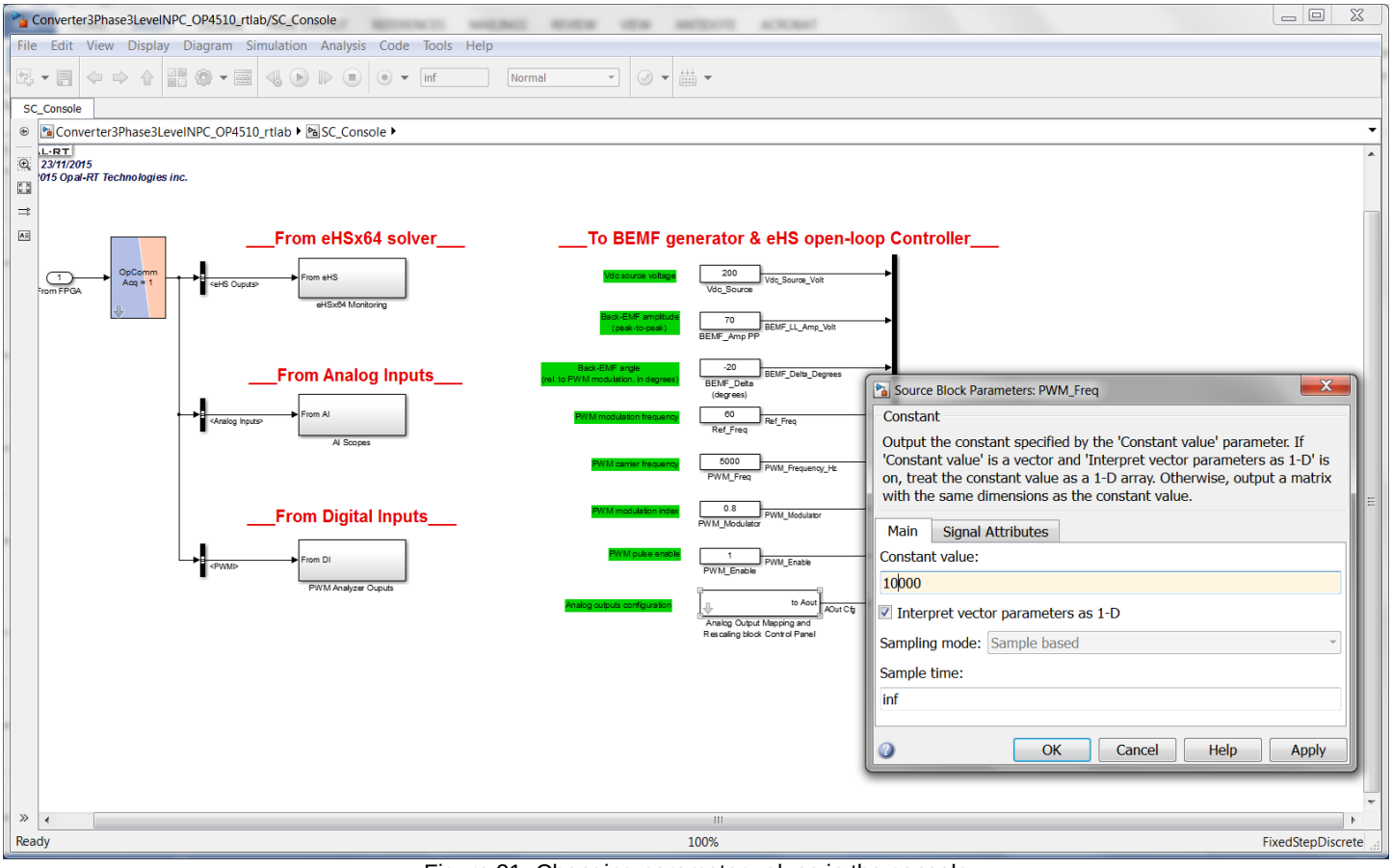


Figure 21: Changing parameter values in the console

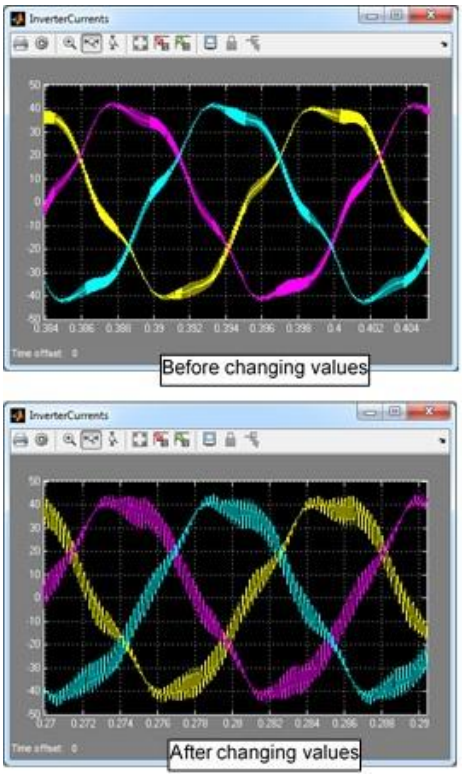


Figure 22: Impact of changing parameter values

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19/05/17