Factory Acceptance Test of a Five-terminal MMC Control and Protection System using Hardware-in-the-loop Method

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***Abstract*—Being the first five-terminal Modular Multilevel Converter (MMC)-based HVDC project in the world, the control and protection system must be validated under various operation modes as well as contingency at the factory acceptance test. This paper presents the configuration and performance of a hardware-in-the-loop (HIL) test platform that is based on a multi-rate real-time simulator using commercial-off-the-shelf architecture. The MMC sub-module model is implemented in field programmable gate array (FPGA) boards with a computation cycle of 500 ns, while the rest of the power system is simulated on the central processing unit (standard multi-core CPU) with a time-step of 30 µs. The State-space Nodal (SSN) interface is used to couple the models simulated on FPGA and on CPU. In addition, a communication protocol based on Giga-bit Ethernet is designed to connect the actual valve balancing controller with the real-time simulator. Results from the factory acceptance test are presented in this paper.**

***Index Terms*—Hardware-in-the-loop (HIL), Modular Multilevel Converter (MMC), Multi-terminal HVDC, Power system simulation, Real-time systems, FPGA simulators.**

I. INTRODUCTION

The Zhoushan Archipelago, located in the East China Sea, consists of more than 1390 islands. Since the islands are distributed like a chain, the structure of the power grid on the islands is limited by the geographical constraint. The fast development in this region requires flexibility and reliability in power supply. In addition, there are rich wind power resources on the islands. As of now, the power grid is not strong enough to integrate the wind power or other distributed energies. In order to strengthen the grid interconnection between the main island and other islands, the China State Grid decided to construct a five-terminal ±200kV MMC-based HVDC project with a total capacity of 1000 MW to enhance the grid reliability. Fig. 1 shows the geographical location of MMC stations. Unlike an AC network, as planned originally, MMC-based HVDC can provide very fast and dynamic support of reactive power according to the variation of the loads. Consequently, the stability of the whole grid is improved and the power quality problems existing in certain areas of the Zhoushan Archipelago can be solved. [1]

Figure 1. The geographical location of the MMC stations

Compared to a two-terminal HVDC system, the control and protection (C&P) schemes in the five-terminal MMC-HVDC system are more complex, because it needs proper coordinated strategy among stations to guarantee the system can keep on operating after a failure [2]. Under the normal operation mode, the Zhoushan station is the only terminal that provides power to the rest of the system. However, a total of 27 operation modes are designed taking onto consideration that one or more terminals may trip due to temporary fault or maintenance [3]. The full C&P system must be validated for all designed operation modes, as well as under fault conditions during the factory acceptance test (FAT). The HIL method, which connects an actual controller in closed loop with the simulator emulating power system and power electronics converter in real-time, has been accepted and applied for the controller FAT in several HVDC projects [4]–[5]. Considering the large number of test cases and safety constraints, a HIL platform becomes the most effective and efficient tool to perform the FAT for the actual C&P system of this five-terminal MMC-HVDC project before field commissioning.

This paper first introduces the architecture of the HIL test platform used in this FAT, then explores the most recently developed MMC and power system model based on the State-space Nodal (SSN) solver, as well as the I/O interface between the real-time model and the actual C&P system under test. In the end, some results obtained at the FAT are presented in this paper.

II. Description of the Test Setup

The C&P system under test consists of four types of controllers, namely, the AC control center (ACC), the DC field terminal (DFT), the pole control and protection (PCP), and the voltage balancing controller (VBC). The ACC and DFT are the high-level control and protection schemes for the AC networks and DC networks respectively. A PCP communicates with the ACC through the MMC substation LAN, and applies the proper control algorithm according to the system operation mode. A VBC receives reference signals from the PCP via the IEC60044-8 protocol, and modulates the firing commands for the IGBTs in each sub-module to equalize the sub-modules capacitor voltages within the valve. In order to test the task switching between the controller on duty and the redundant controller, two sets of controllers are connected to the RT-LAB HIL test bench selected as the HIL test platform. Fig. 2 depicts the setup for the FAT of one MMC terminal. Several OP7020 FPGA MMC simulators are interconnected through the PCI express switch to simulate the five HVDC terminals.

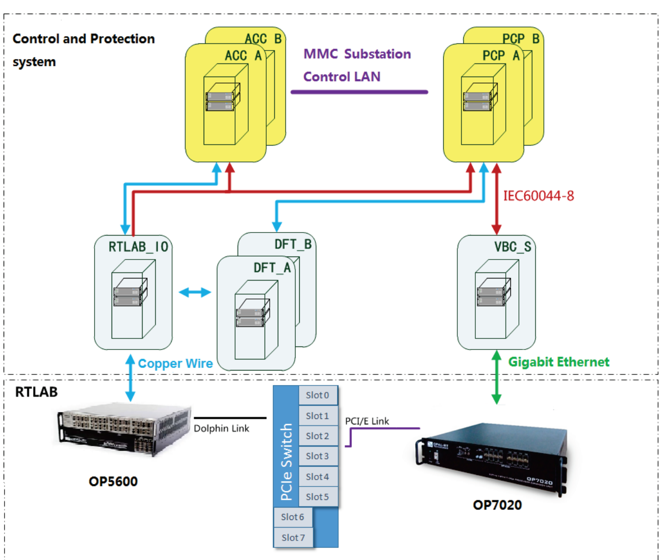

Figure 2. HIL Setup for one MMC terminal

A. *Real-time Simulator*

The RT-LAB real-time simulator adopts commercial off-the-shelf structure. It simulates the MMC valve model in VIRTEX-7 FPGA using 500 nanoseconds time step, while the AC networks are simulated on the standard processor. The OP5600 is equipped with two 3.4 GHz Intel i7 6-core processors and a Xilinx Spartan-3 FPGA chip, whose I/O pins are physically routed to a carrier board mounted with signal conditioning modules. These modules can be either digital-to-analogue converters (DAC) to send the measured voltages and currents to the actual controller under tests, or optically isolated digital modules to receive circuit breaker commands and send the circuit breaker positions. The OP7020 is a compact Virtex-7™ FPGA-based simulator and accommodates 16 high-speed fiber optic modules (SFP) that can communicate with a VBC directly. The OP7020 is particularly optimized for the real-time simulation of 3000 MMC sub-modules with a time-step less than 500 ns. The platform used for this FAT consists of two OP5600s and five OP7020s that are connected together through a PCI Express (PCIe) switch.

B. *HIL Interface*

The MMC C&P system consists of several cascaded controllers. The ACC, DFT and PCP are generally considered as high-level controllers, while the VBC and the sub-module controllers (SMC) are classified as low-level controllers.

The high-level controllers acquire the voltages and currents at both sides of the grid-coupling transformer, as well as the DC voltage and current for each terminal. Those measurements are directly available from the analog outputs of the OP5600. Although an I/O mapping and conditioning cabinet is required to adapt and route those signals received from the simulator to the high-level controllers, the HIL interface is still affordable in terms of cost and effort.

However, the low-level controllers use at least one pair of optical fibers to communicate with each sub-module. In this project, each MMC has 270 sub-modules per valve, hence 1620 sub-modules in total. Considering that five C&P systems will be tested at the same time, there are thousands of optical fibers to connect, which requires a lot of time and effort. Alternatively, the SMCs can be emulated on the FPGA with the sub-modules model. In this case, only one or two pairs of optical cables are required for the bi-directional communication between the VBC per valve. Thanks to the flexibility given by the OPAL-RT RT-XSG toolbox, the user can customize the data frame on the top of the Gigabit Ethernet protocol. Therefore, the original communication link between the VBC and SMC can be used in the FAT, so that the HIL test can maintain its fidelity with minimum effort and cost.

In this test, two pairs of optical fiber links per valve are used to communicate between the VBC and the OP7020. Each link carries the data for 135 sub-modules. The message format complies with the standard frame specified by the IEEE 802.3 [6]. The media of communication is multimode fiber (MMF) running Gigabyte Ethernet protocol. The simulated SMC will send the valve current, capacitor voltages of sub-modules, as well as fault flags for each sub-module, which identify different types of faults or malfunctions occurring in the sub-module, such as over-voltage, over-current or power failure. According to the fault flag, the VBC can decide to either temporally or permanently bypass the sub-module. In normal operation, the VBC samples the capacitor voltages of each sub-module every tens of microseconds, and then send the firing command to each IGBT to charge or discharge a sub-module for a VBC control cycle to ensure balanced capacitor voltages within the valve. Since the data are transmitted between the simulated SMC and the real VBC in series, special precautions must be taken about the synchronization among the 12 communication links for the same MMC. Particularly, the simulated SMC should not dispatch the firing pulses to the IGBT model until the whole packet of messages for each MMC valve is completely transmitted at a certain VBC control cycle. Otherwise, an incomplete packet, or a packet of data concatenated by two frames of the consecutive control cycle will lead inaccuracy in the simulation.

The message sending from the simulator to the VBC is composed to follow the data frame shown in Table I, while the communication frame in the opposite direction is defined in Table II and III. This communication protocol is open and can therefore be used by any customer.

TABLE I. COMMUNICATION FRAME FROM SMC TO VBC

Content	Length (Bytes)	Note
Destination MAC	6	Configurable
Source MAC	6	Configurable
Nb. of sub-moduels	2	Configurable
Sub-moduel info	1120	12 bits for capacitor voltage and 28 bits for the fault flag of each SM[a]
Arm current	2	Signed fixed point number
Data Type	2	Reserved
CRC	4	Polynomial is 0x4C11DB7

[a] The data frame is designed for maximum 224 sub-modules, and the data will be sent from the SM1 to SM224. If the number of SMs is less than 224, 0x0000000000 will be filled into the place.

TABLE II. COMMUNICATION FRAME FROM VBC TO SMC

Content	Length (Bytes)	Note
Destination MAC	6	Configurable
Source MAC	6	Configurable
Nb. of sub-moduels	2	Configurable
Firing control command	996	2 bytes for each SM, the length is reserved for 224 SMs
Data Type	2	Reserved
CRC	4	Polynomial is 0x4C11DB7

TABLE III. CONTENT OF FIRING CONTROL COMMAND

Bit	Data	Definition
Bit 0	IGBT_upper	Upper IGBT fired
Bit 1	IGBT_lower	Lower IGBT fired
Bit 2	DLC	Bypass switch close
Bit 3	SCR	Thyristor fired
Bit 4	Rsv	Reserved
Bit 5	Dblk	Sub-module firing enabled
Bit 6 - 15	Rsv	Reserved

C. *Real-time Simulation Model*

Besides the five MMC terminals and the interconnected DC networks, all 18 substations above 110 kV, including two groups of generators are simulated in real time. Fig. 3 shows the single-line diagram of the power grid used to perform the HIL test of the Zhoushan MMC C&P system. The parameters of each MMC substation are given in Table IV.

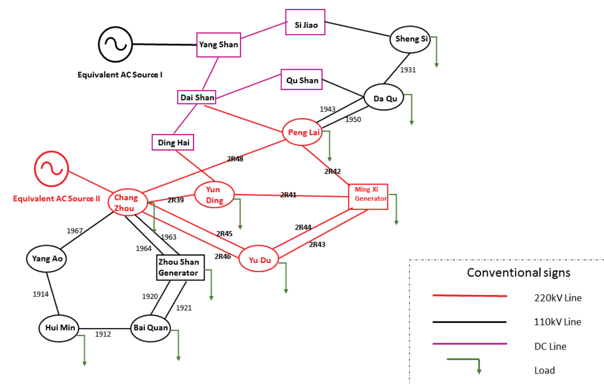

Figure 3. Single-line diagram of the simulated Zhoushan grid

TABLE IV. PARAMETERS OF MMC SUBSTATIONS

Parameters	Ding Hai	Dai Shan	Qu Shan	Yang Shan	Si Jiao
Transfomer connection	Y/D	Y/D	Y/Y	Yn/Y	Y/Y
Rated power (MVA)	400	300	100	100	100
Primary voltage (kV)	230	230	115	115	115
Secondary voltage (kV)	205.1	204.1	208.2	208.2	208.2
Leakage inductance (mH)	15%	15%	14%	14%	14%
Taps	1-15	1-15	1-15	1-15	1-15
Arm Inductance (mH)	90	120	350	350	350
DC inductance (mH)	20	20	20	20	20
Number of SMs per valve	270	270	270	264	264

The real-time simulation model is prepared using a graphical modeling tool, the SimPowerSystems (SPS) blockset in MATLAB. The models of AC equivalent sources, synchronous generators, as well as lumped-parameter passive components (resistors, inductors, and capacitors) come from the SPS, which uses the state-space method to build the mathematical equations. The On-load Tap Changer (OLTC) transformers and the wide-band line used to simulate the underwater cable are modeled using the classic nodal method. The MMC sub-modules are calculated in the FPGA using the mathematical model explained in [5], and represented as an equivalent circuit as shown in Fig. 4. In this equivalent circuit, the MMC valve stays in blocking mode, when T1 is open, and T2 is closed. The MMC valve is in de-blocking mode, if T1 is closed and T2 is open. The time step of the FPGA model was 500 nanoseconds.

RT-LAB real-time simulator uses an advanced solver called State-space nodal (SSN) [7], which enables naturally coupling the state-space models and nodal models into a global admittance matrix [8]. Practically, the Nodal Interface Block (NIB) will be used to split the model into several SSN groups in the Simulink environment. Fig. 5 illustrates how the SSN groups are defined for a single MMC terminal.

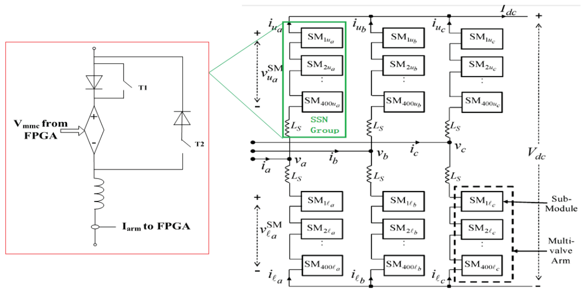

Figure 4. Equivalent circuit of MMC valve

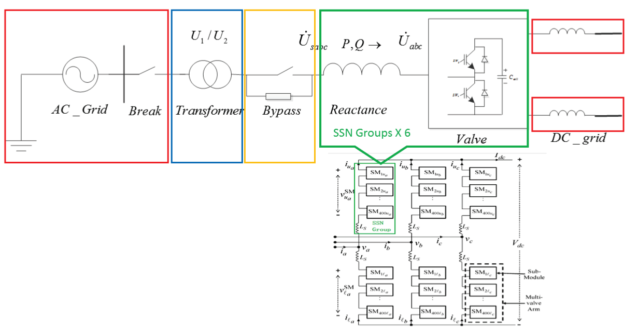

Figure 5. SSN groups in a single MMC station model

For an SSN group that consists of state-spaced models, the group is discretized using higher order matrix exponential approximants, and is derived for its equivalent circuit. The SSN group that contains a nodal model can also be derived from nodal analysis and combined with the state-space equivalent circuits. Using ARTEMIS-SSN makes it possible to increase the size of the circuit to about 400 to 600 nodes without adding inaccuracy introduced by artificial delays.

III. Test Cases

The test cases are designed to cover the scenarios that the MMCs are operated under different control modes, as well as a variety of load conditions, such as the peak power consumption time in summer. Particularly, the C&P systems are examined repetitively for their dynamic responses under contingency. The objective is to evaluate the ride-through capability of MMC according to the pre-defined code and standards, and the coordination among multiple terminals in case of critical failure. This paper presents an example of a single-phase-to-ground fault test case occuring near the primary side of the coupling transformer in the Dinghai station, called F11, when all five terminals are in operation. It should be noted that the Dinghai MMC station is the only station that controls the DC voltage before the fault and delivers power to the other 4 stations. In the first test, the fault duration is 100 ms (Fig 6), while several other tests were performed with fault duration up to 2000 ms as shown in Fig 7.

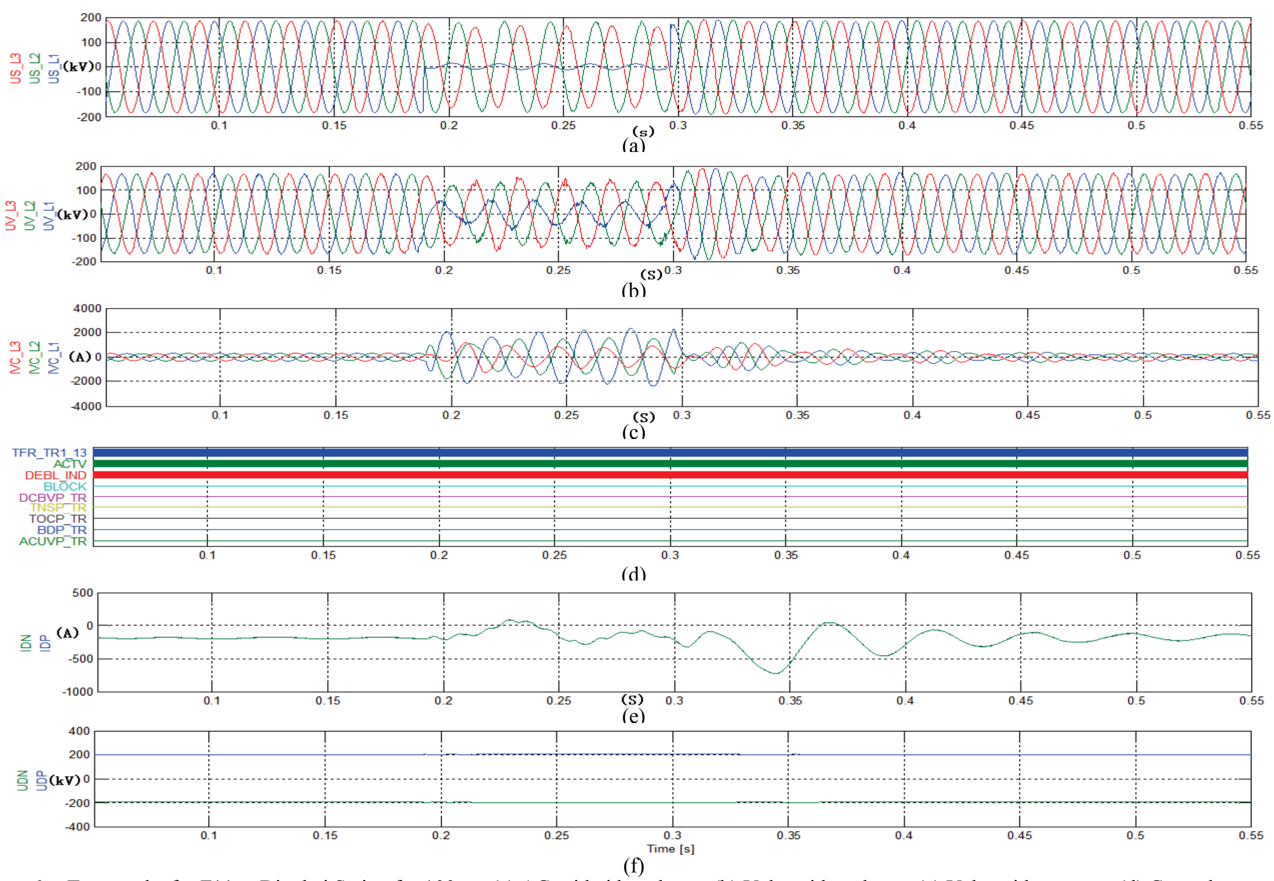

Figure 6. Test results for F11 at Dinghai Staion for 100 ms (a) AC grid-side voltages (b) Valve-side voltages (c) Valve-side currents (d) Control status (e) DC currents (f) DC voltages

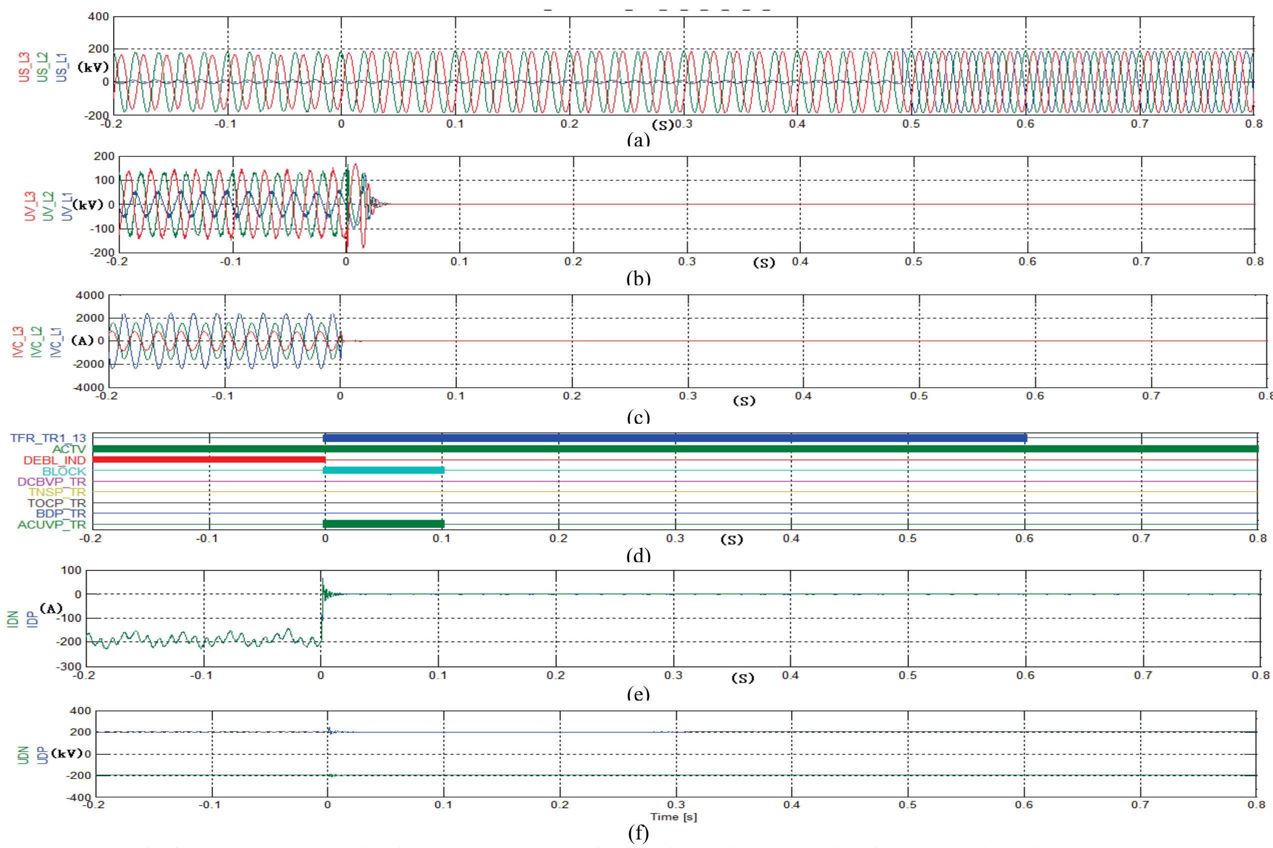

Figure 7. Test results for F11 at Dinghai Staion for 2000 ms (a) AC grid-side voltages (b) Valve-side voltages (c) Valve-side currents (d) Control status (e) DC currents (f) DC voltages

In the first test (fig. 6), the MMC station successfully rides through the F11 fault for 100 ms. The DC voltage can maintain stable during the fault, while the AC voltages recover to normal values about 0.1 s after clearance of the fault. In the second test, the MMC station blocks itself and then trips its circuit breaker due to AC under-voltage protection (ACUVP_TR) after the fault lasts for more than 0.1 s. However, the DC voltage can still remain stable, even if the MMC station dedicated to control the DC voltage trips. The overall performance of the C&P system under the FTP complies with the engineering standard of this project.

I. Conclusions

This paper presents an HIL test bench used in the FAT of the C&P systems of Zhoushan five-terminal MMC-HVDC project. A cost-effective interface based the Gigabit Ethernet protocol is designed to address the challenge of massive I/O connection between the VBC and the real-time simulator. Detailed MMC valve model implemented FPGA with a time step of 500ns provides high precision in gating signals timing. The advanced SSN solver is used to simulate various models for electrical components that are mathematically modelled by different methods. The presented multi-FPGA/CPU based HIL platform provides efficient and economical method to validate the C&P system according to the engineering standards. The C&P system of the Zhoushan five-terminal MMC system finally passed the FAT and was successfully commissioned in the field.

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